

FIG. 1

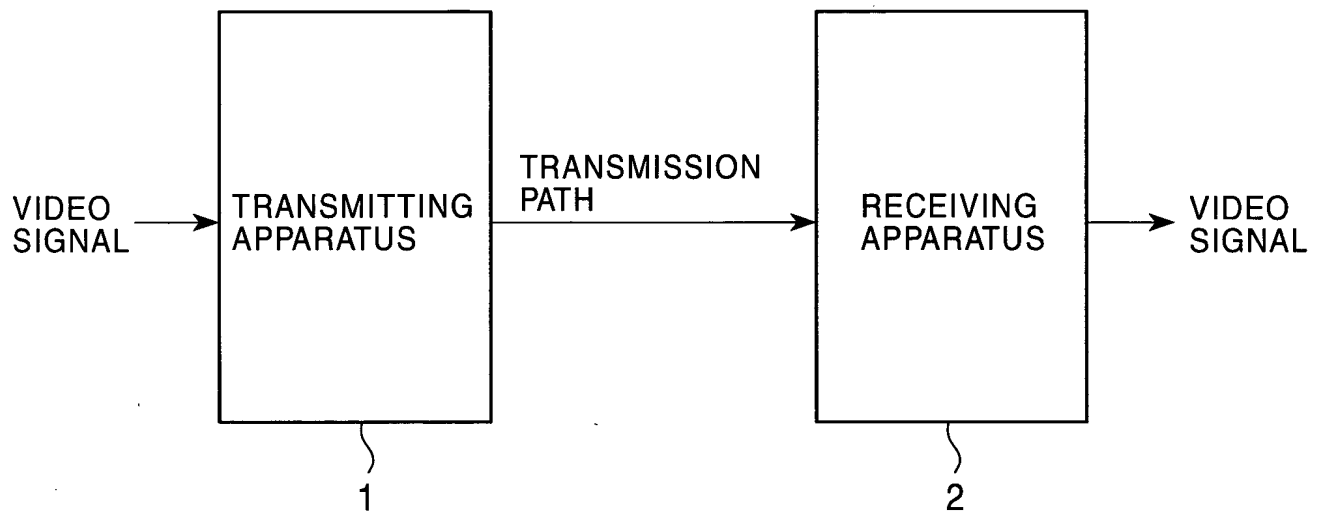


FIG. 2

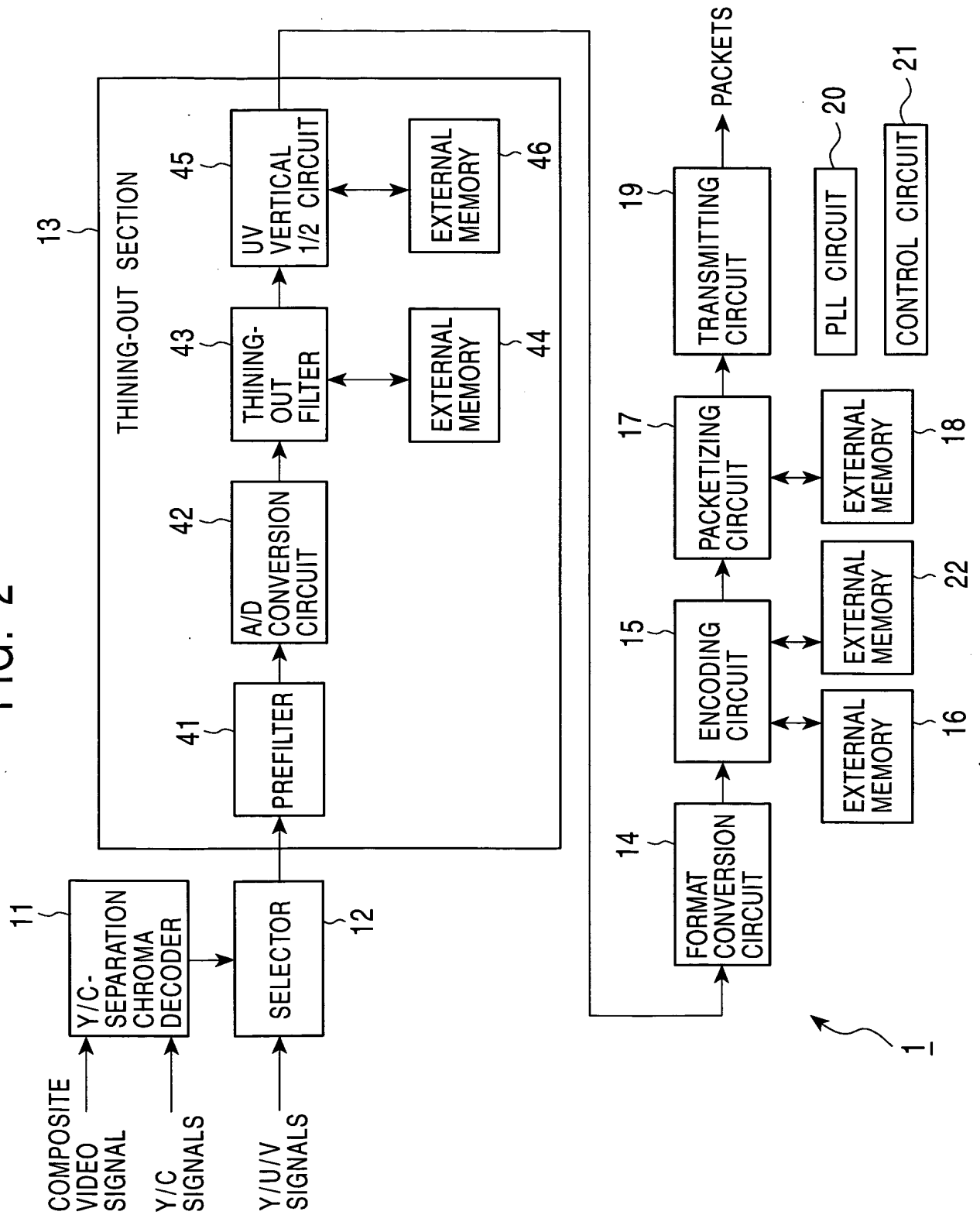


FIG. 3

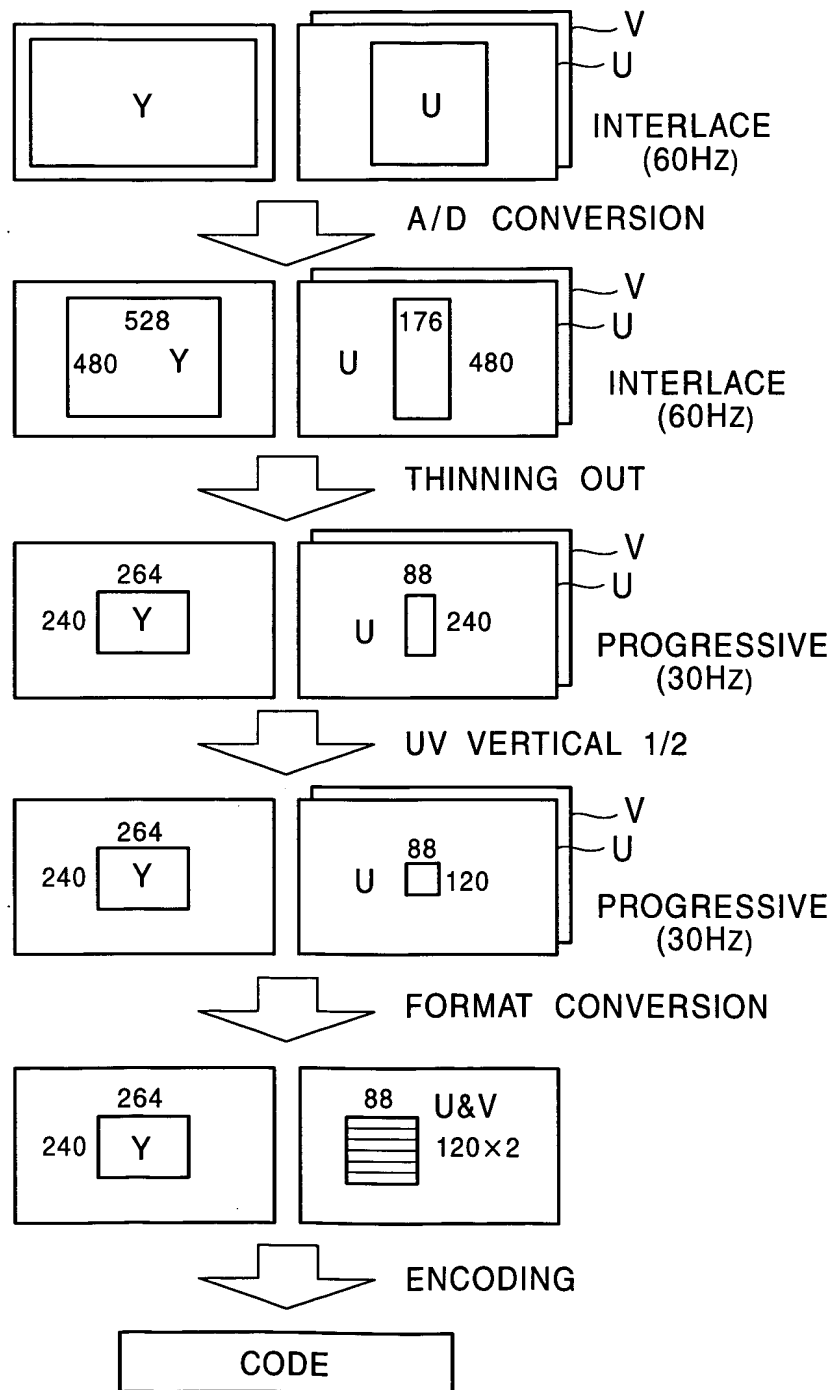


FIG. 4

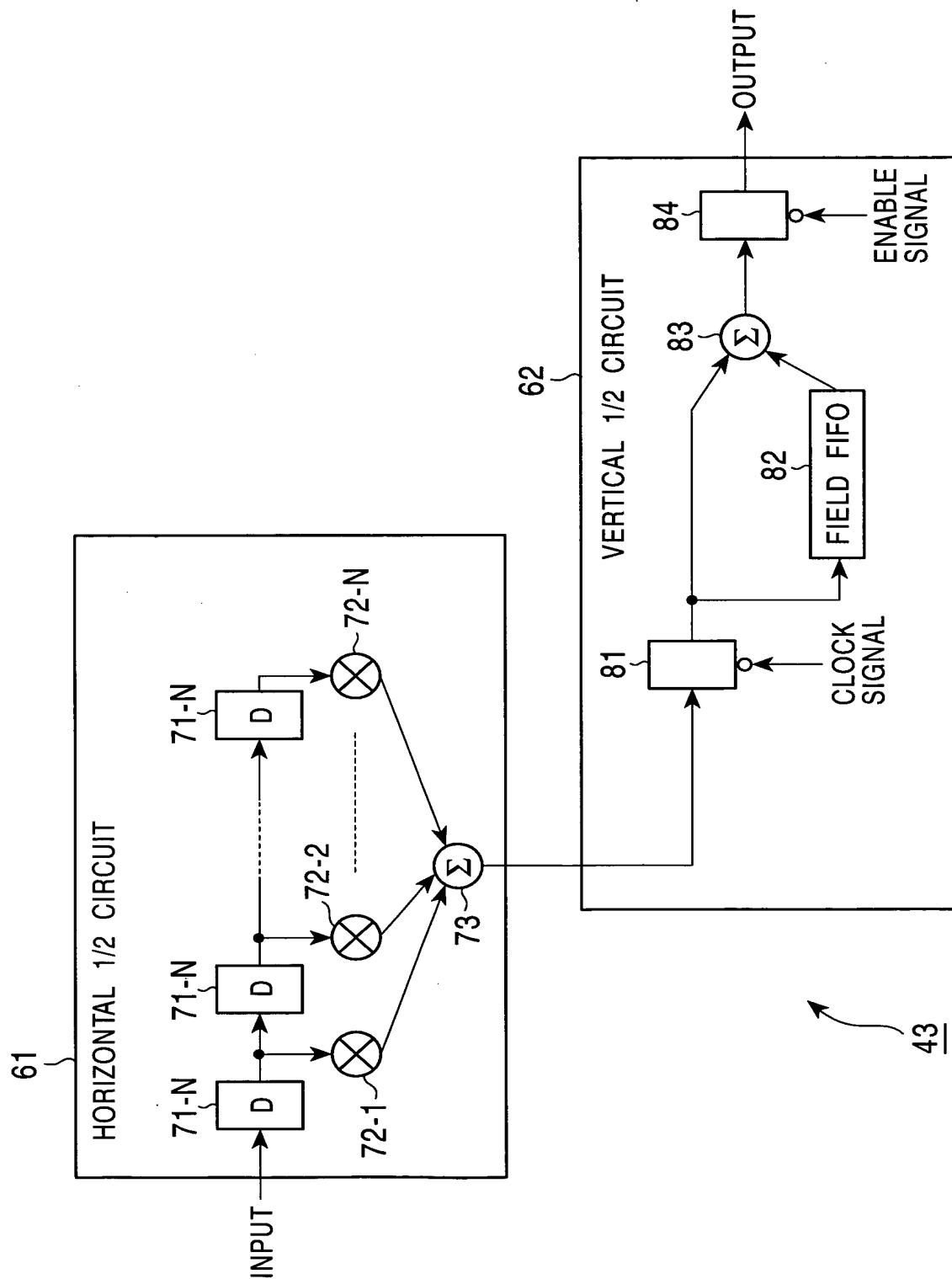


FIG. 5

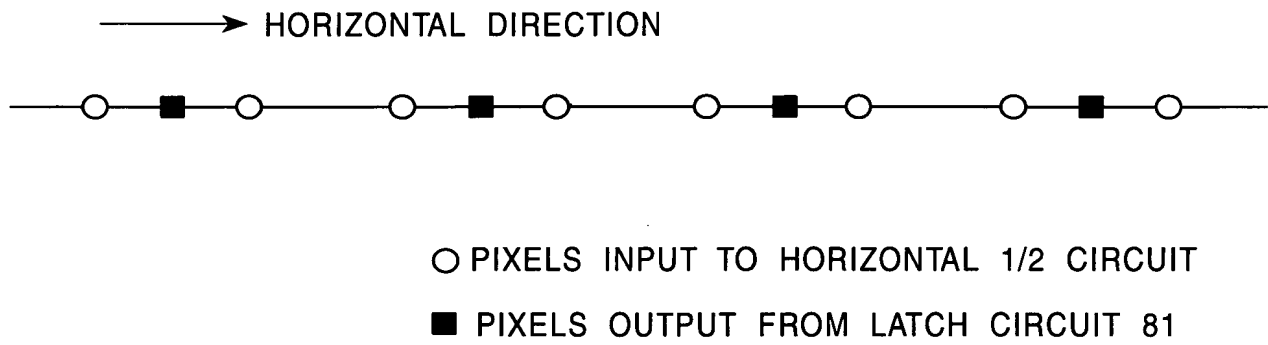
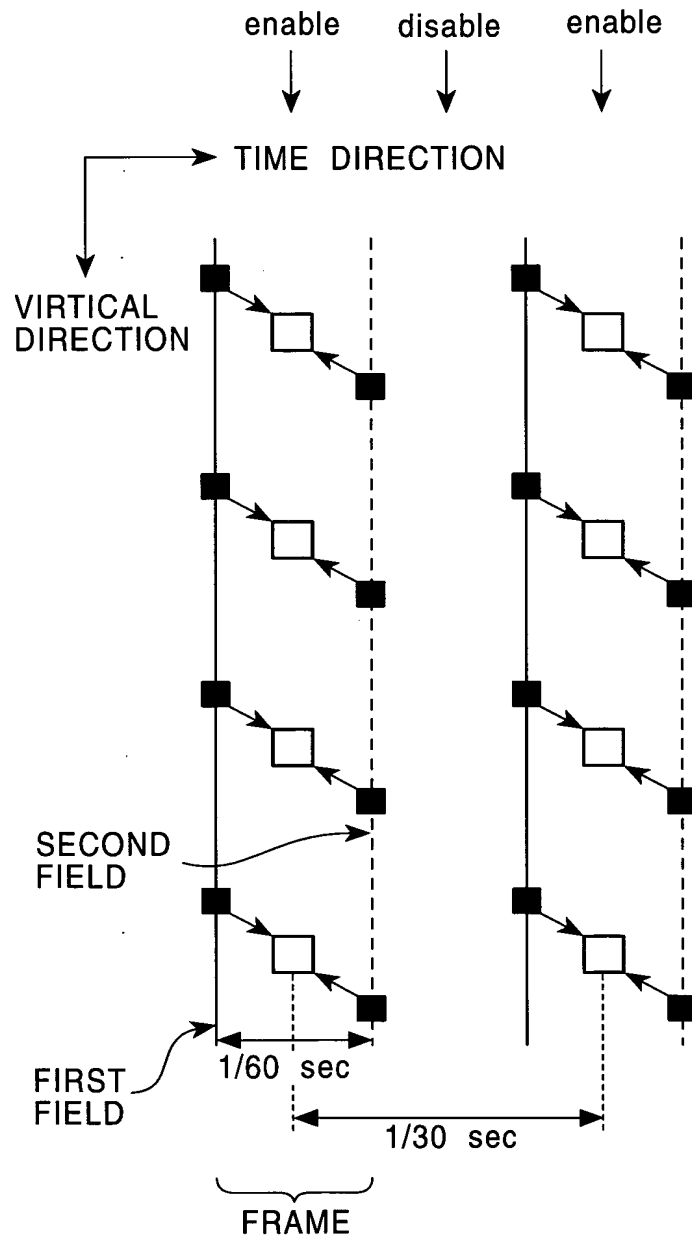


FIG. 6



■ PIXELS OUTPUT FROM LATCH CIRCUIT 81

□ PIXELS OUTPUT FROM LATCH CIRCUIT 84

FIG. 7

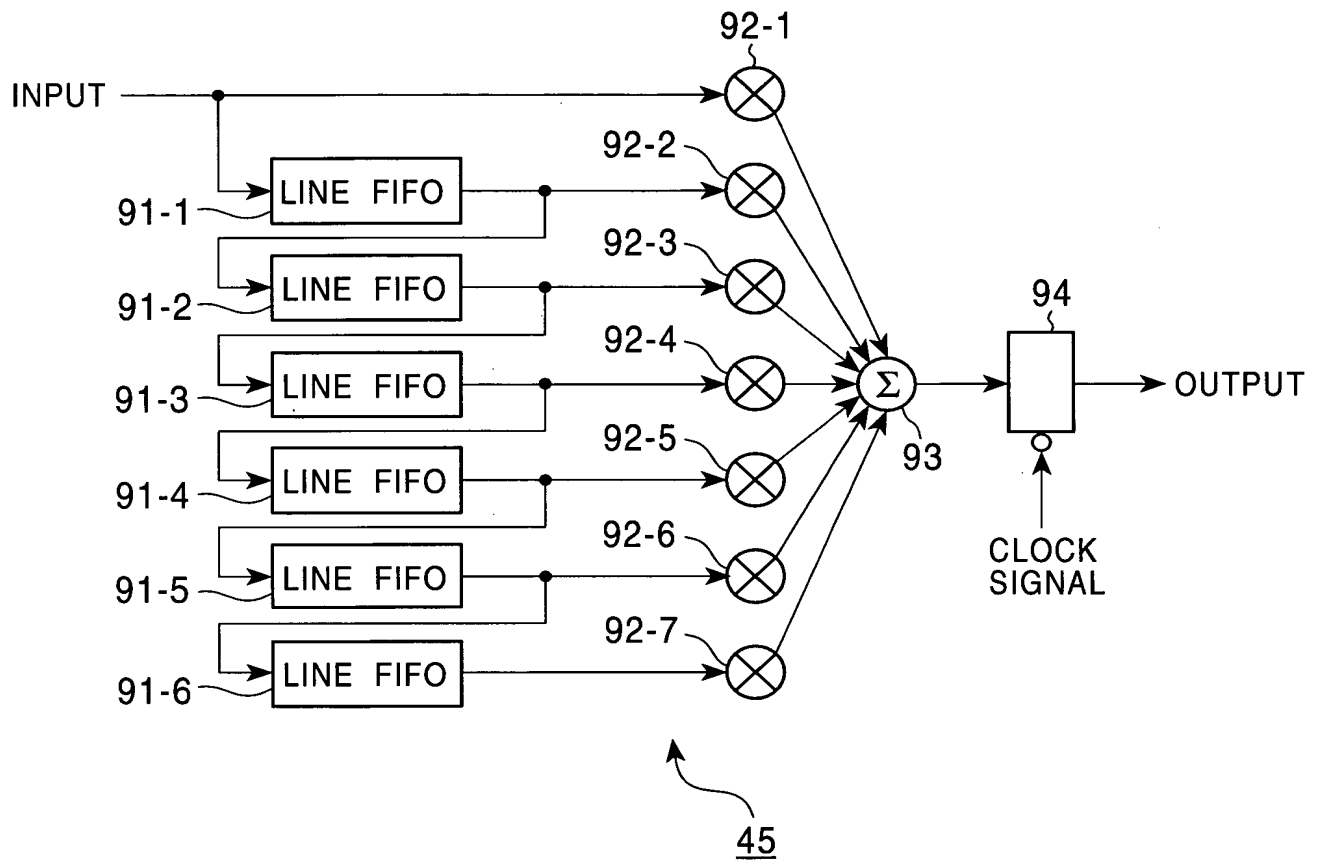
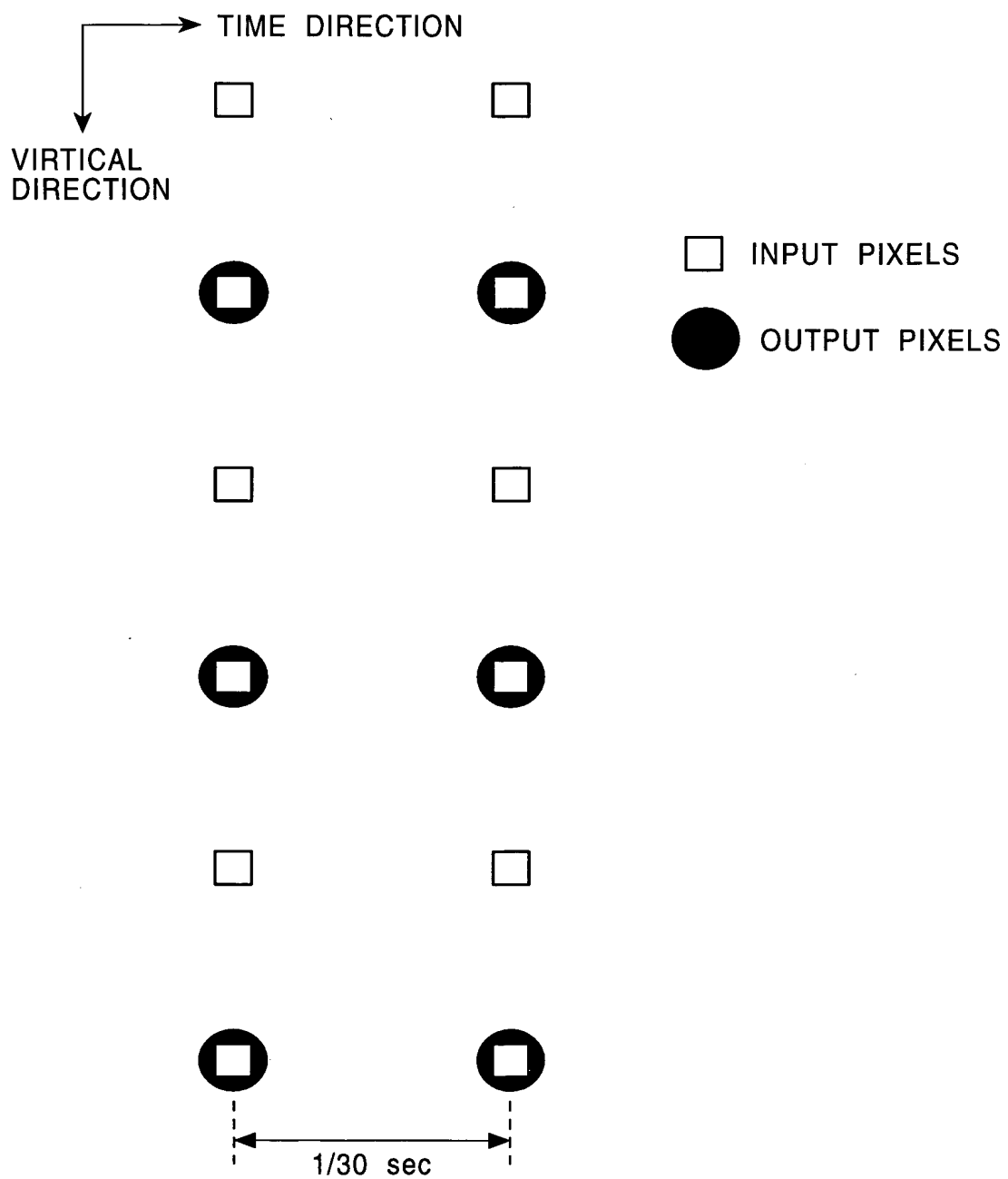


FIG. 8



1128020-020804

FIG. 9

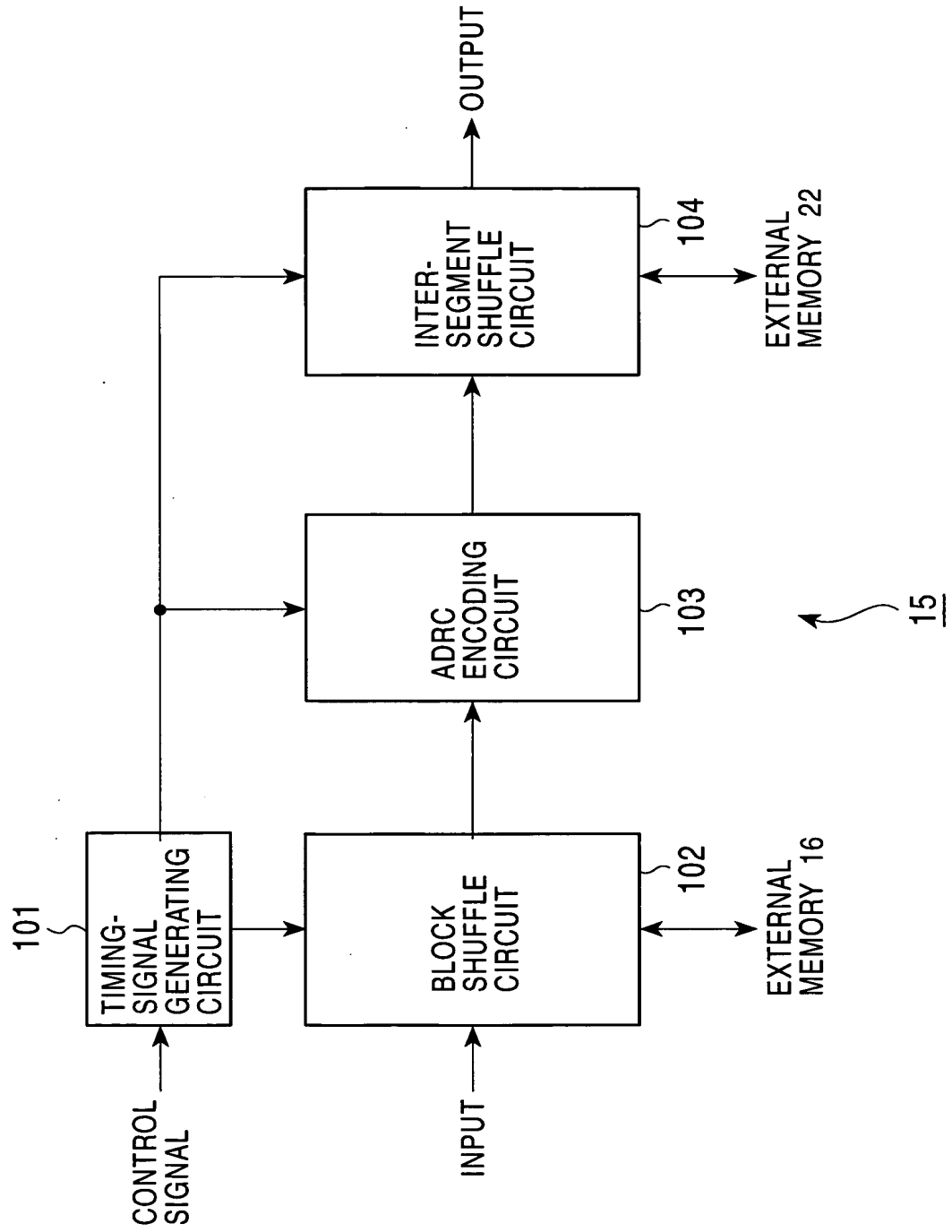


FIG. 10

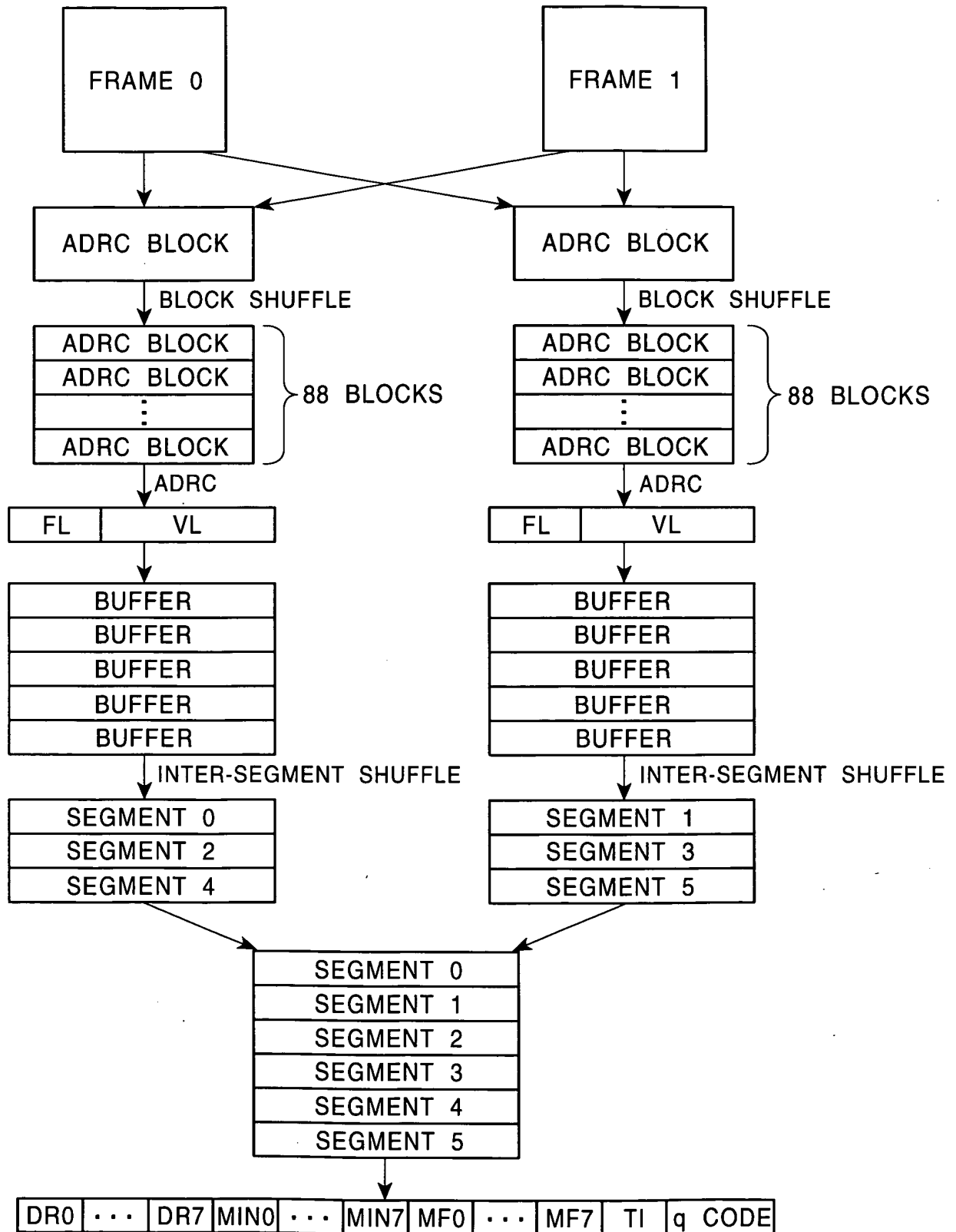


FIG. 11

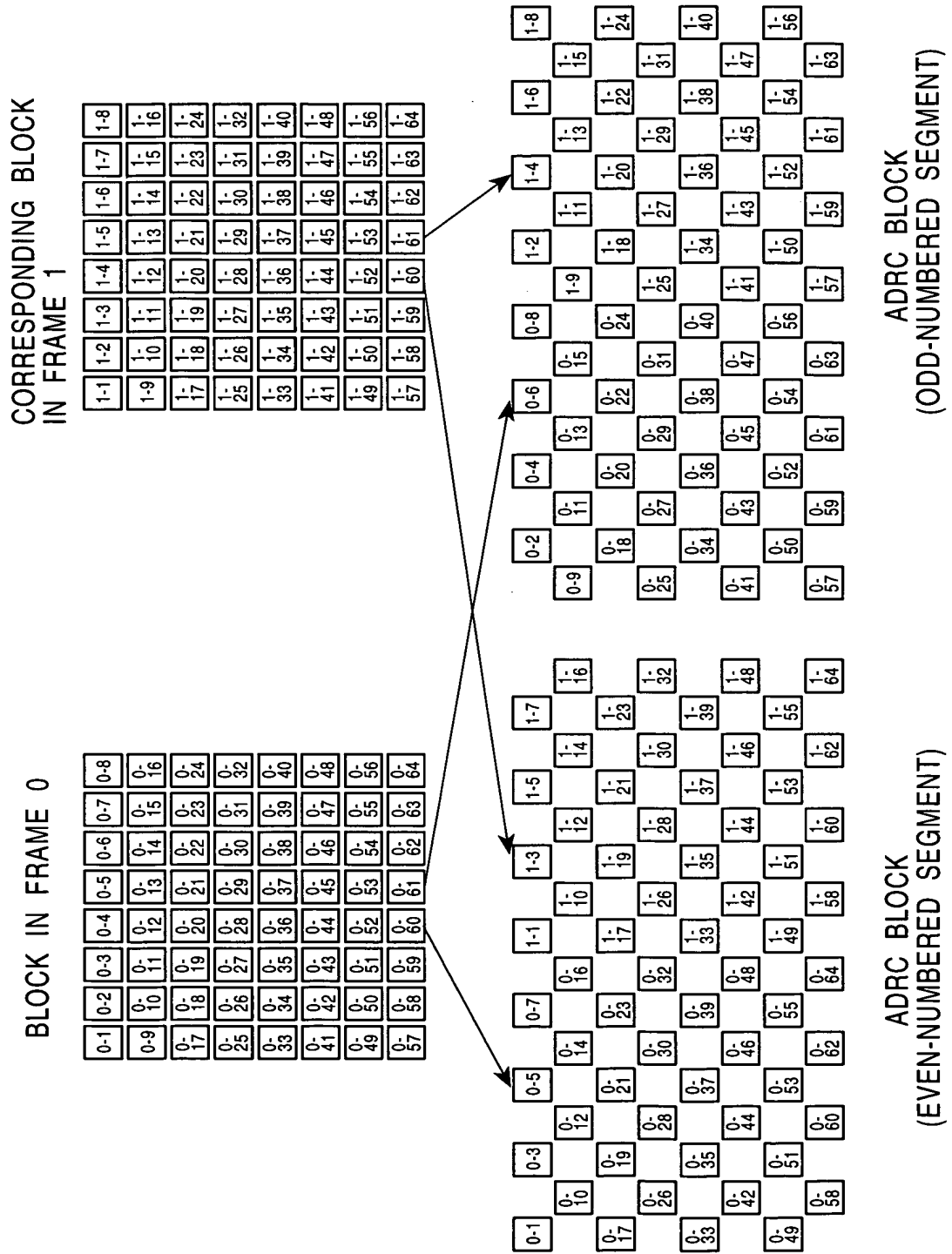


FIG. 12

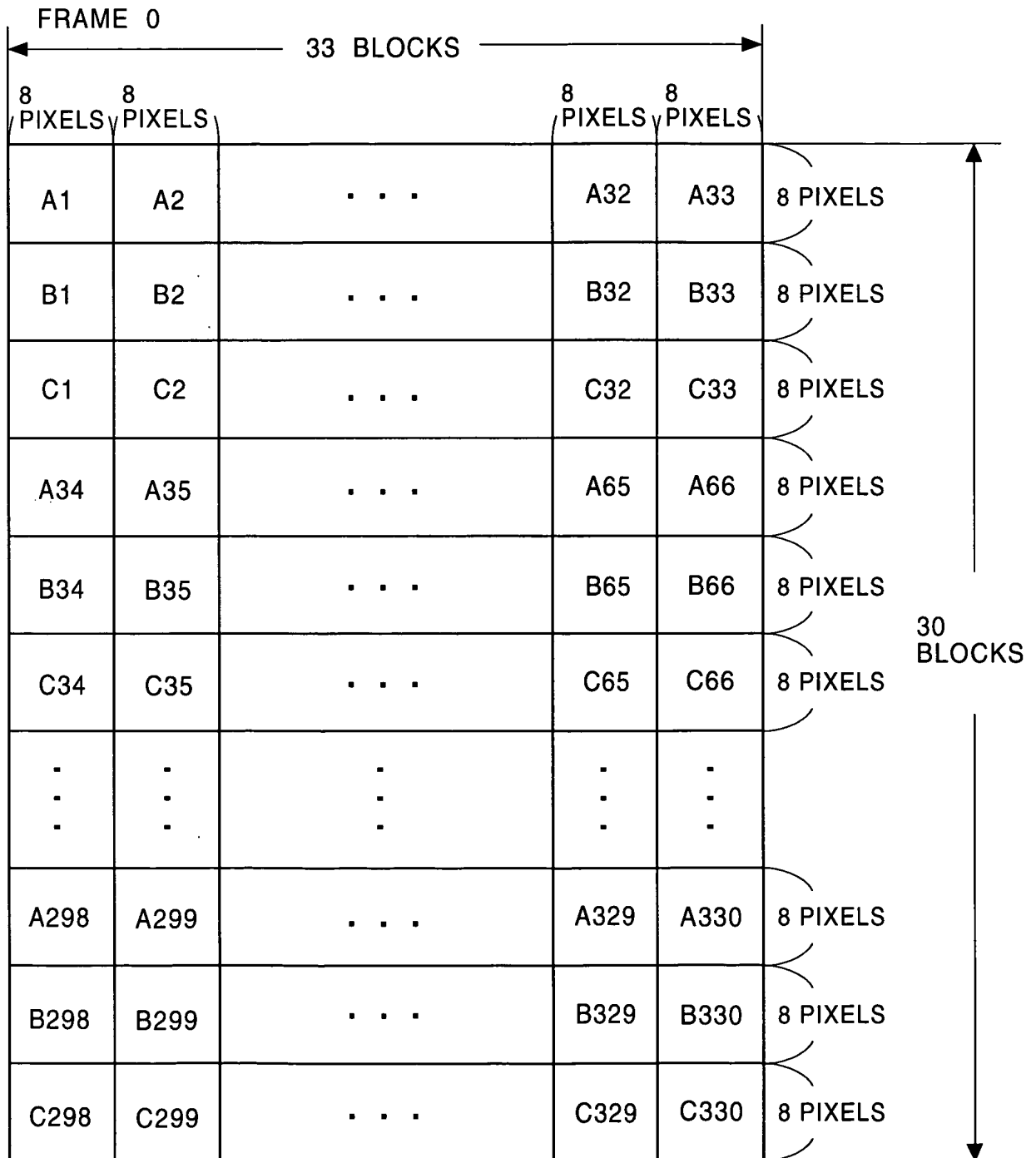


FIG. 13

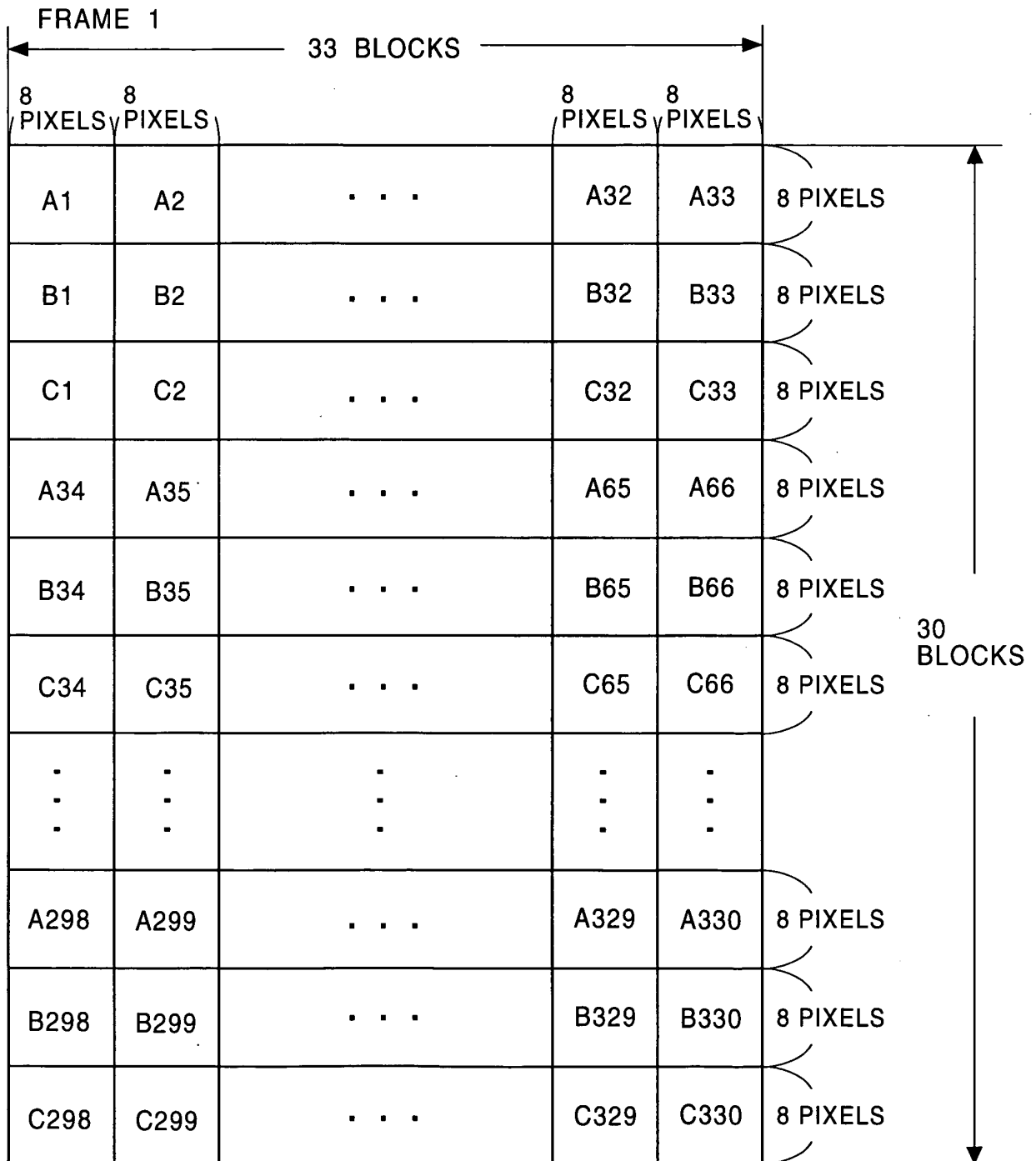


FIG. 14

ADRC BLOCK 0	ADRC BLOCK 3	ADRC BLOCK 0	ADRC BLOCK 3
ADRC BLOCK 4	ADRC BLOCK 1	ADRC BLOCK 4	ADRC BLOCK 1
ADRC BLOCK 2	ADRC BLOCK 5	ADRC BLOCK 2	ADRC BLOCK 5
ADRC BLOCK 0	ADRC BLOCK 3	ADRC BLOCK 0	ADRC BLOCK 3
ADRC BLOCK 4	ADRC BLOCK 1	ADRC BLOCK 4	ADRC BLOCK 1
ADRC BLOCK 2	ADRC BLOCK 5	ADRC BLOCK 2	ADRC BLOCK 5

...

...

FIG. 15A

ORIGINAL SCREEN

66 ADRG BLOCKS

30 ADRG BLOCKS

0	3	0	3	0	3	0	3		0	3
4	1	4	1	4	1	4	1		4	1
2	5	2	5	2	5	2	5		2	5
0	3	0	3	0	3	0	3		0	3
4	1	4	1	4	1	4	1		4	1
2	5	2	5	2	5	2	5		2	5
0	3	0	3	0	3	0	3		0	3
4	1	4	1	4	1	4	1		4	1
2	5	2	5	2	5	2	5		2	5

FIG. 15B

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

0	0	0	0	0	0	0	0		0	0
0	0	0	0	0	0	0	0		0	0
0	0	0	0	0	0	0	0		0	0

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

1	1	1	1	1	1	1	1		1	1
1	1	1	1	1	1	1	1		1	1
1	1	1	1	1	1	1	1		1	1

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

2	2	2	2	2	2	2	2		2	2
2	2	2	2	2	2	2	2		2	2
2	2	2	2	2	2	2	2		2	2

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

3	3	3	3	3	3	3	3		3	3
3	3	3	3	3	3	3	3		3	3
3	3	3	3	3	3	3	3		3	3

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

4	4	4	4	4	4	4	4		4	4
4	4	4	4	4	4	4	4		4	4
4	4	4	4	4	4	4	4		4	4

SEGMENT

33 ADRG BLOCKS

10 ADRG BLOCKS

5	5	5	5	5	5	5	5		5	5
5	5	5	5	5	5	5	5		5	5
5	5	5	5	5	5	5	5		5	5

FIG. 16B

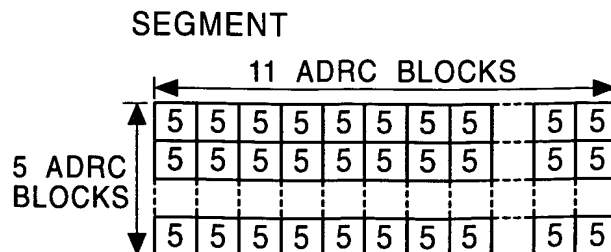


FIG. 17A

y0	y1	y2	y3	y4	y32
y33	y34	y35	y36	y37	y65
y297	y298	y299	y300	y301	y329

FIG. 17B

y0	y221	y112	y3	y224	y142
y33	y254	y145	y36	y257	y175
y297	y188	y79	y300	y191	y109

FIG. 17C

u0	u1	u2	u3	u4	u10
u11	u12	u13	u14	u15	u21
u44	u45	u46	u47	u48	u54

FIG. 17D

u54	u53	u52	u51	u50	u44
u43	u42	u41	u40	u39	u33
u10	u9	u8	u7	u6	u0

FIG. 17E

v0	v1	v2	v3	v4	v10
v11	v12	v13	v14	v15	v21
v44	v45	v46	v47	v48	v54

FIG. 17F

v54	v53	v52	v51	v50	v44
v43	v42	v41	v40	v39	v33
v10	v9	v8	v7	v6	v0

FIG. 18

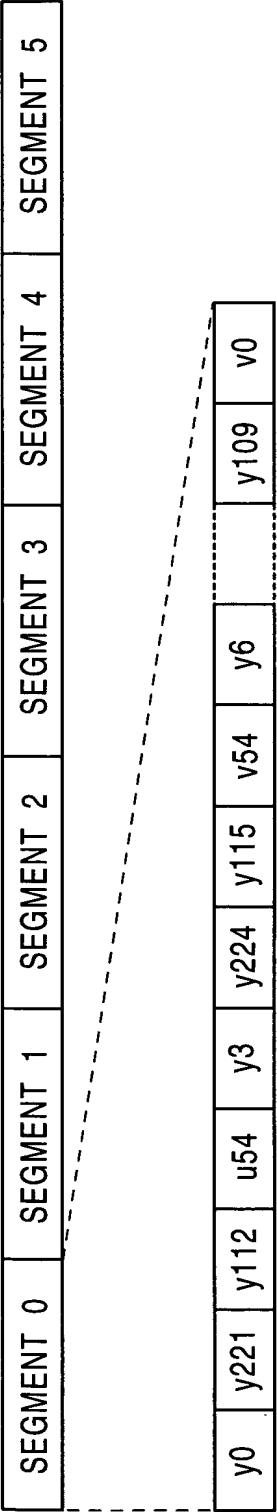


FIG. 19

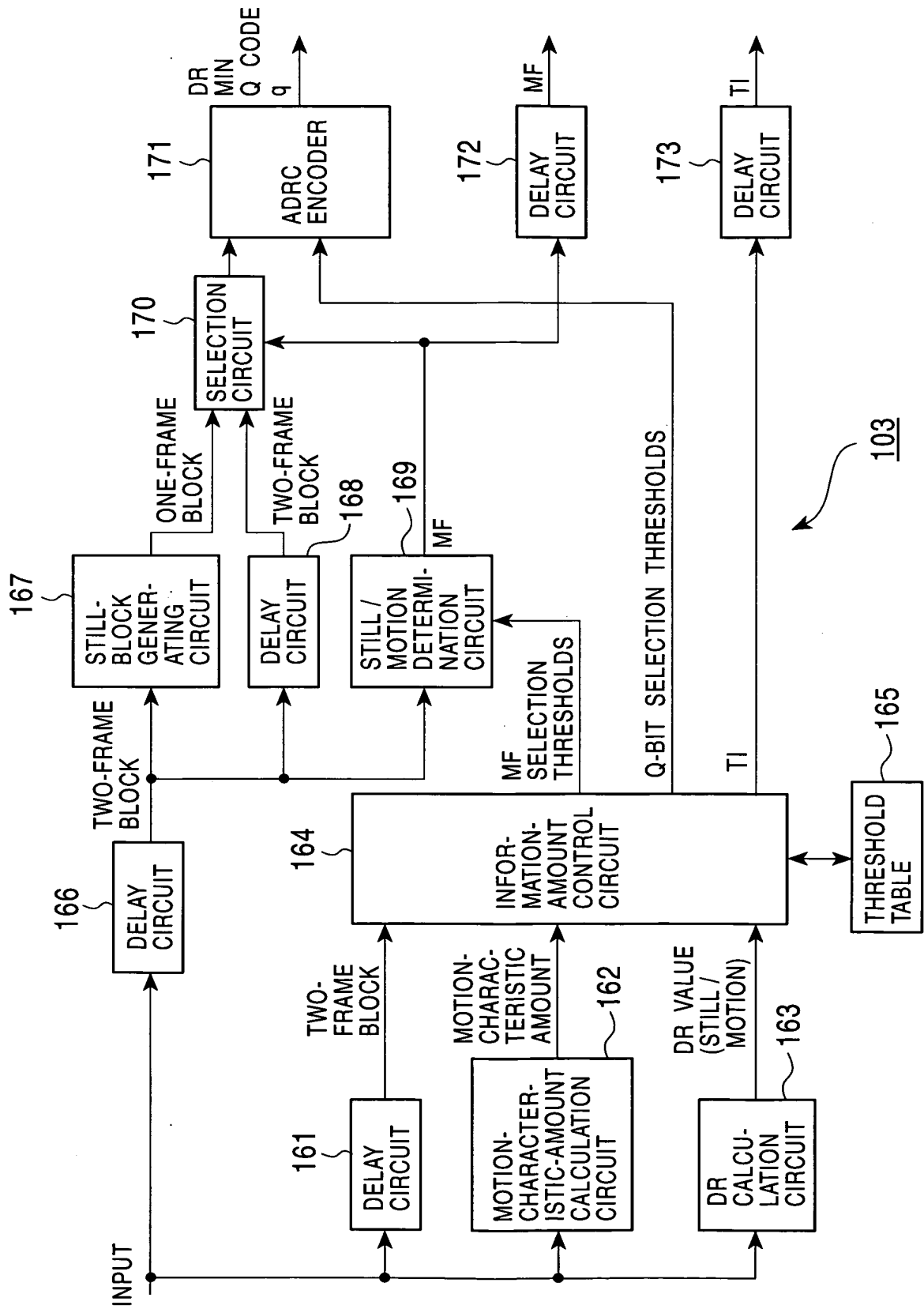


FIG. 20

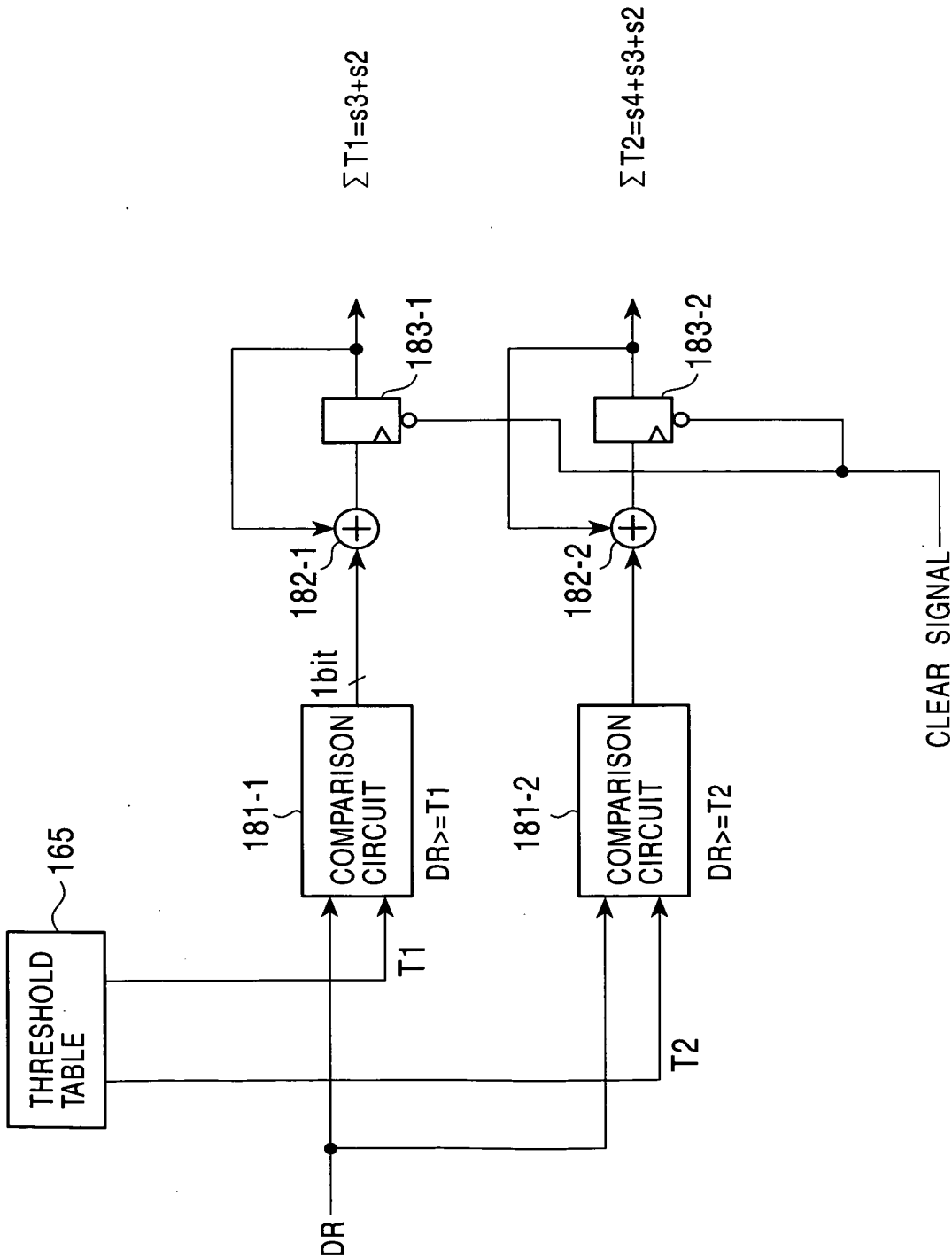


FIG. 21

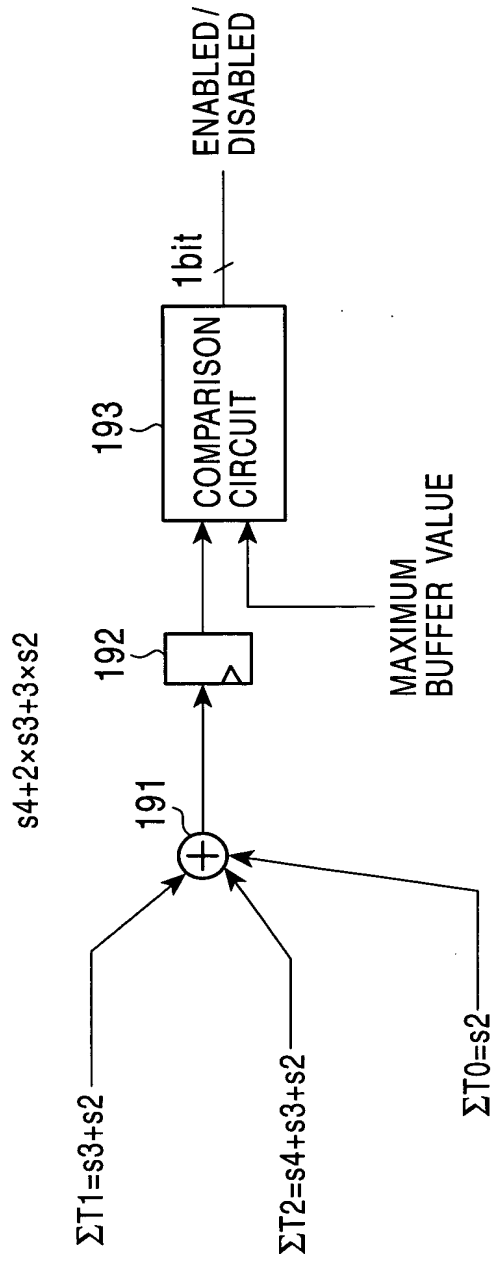


FIG. 22

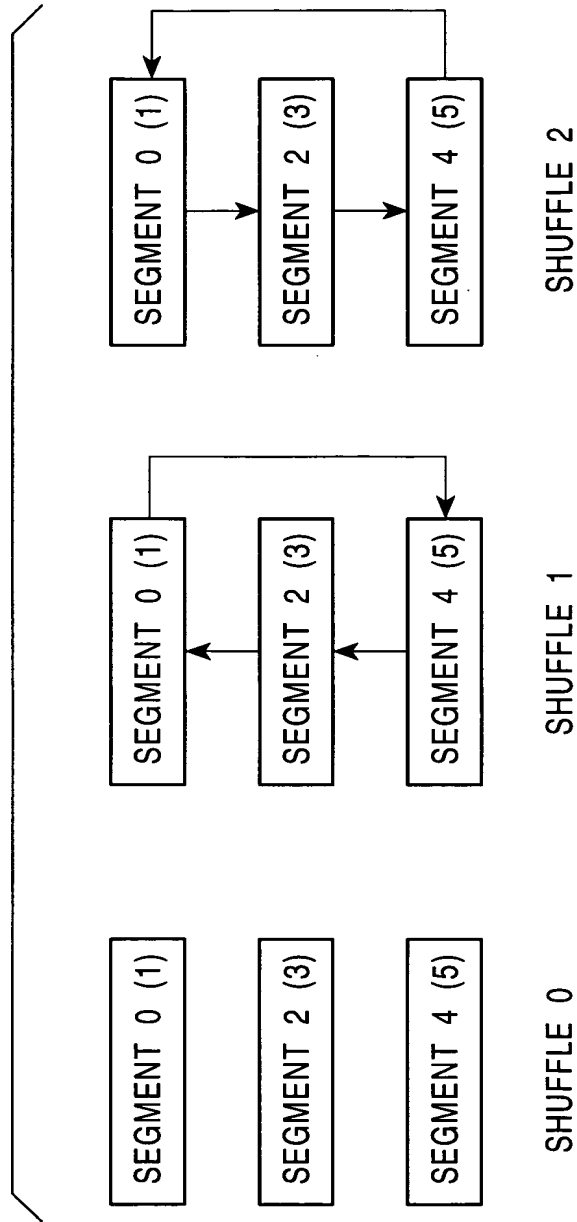


FIG. 23

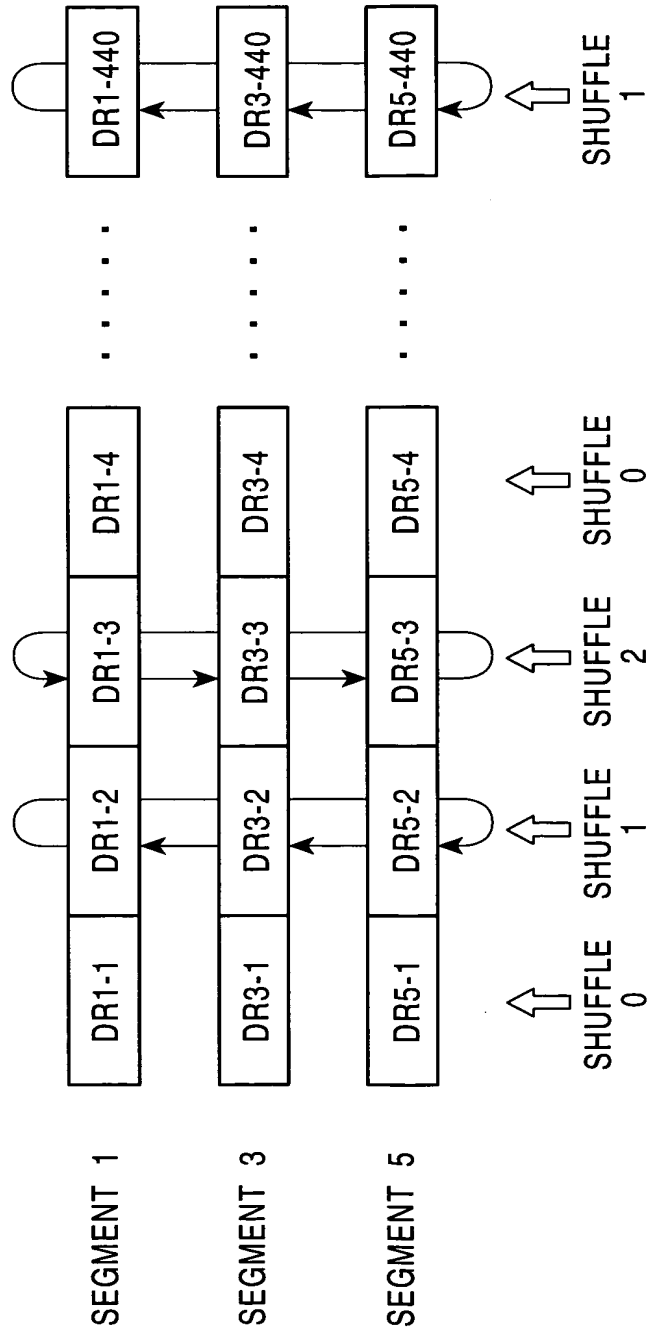


FIG. 24

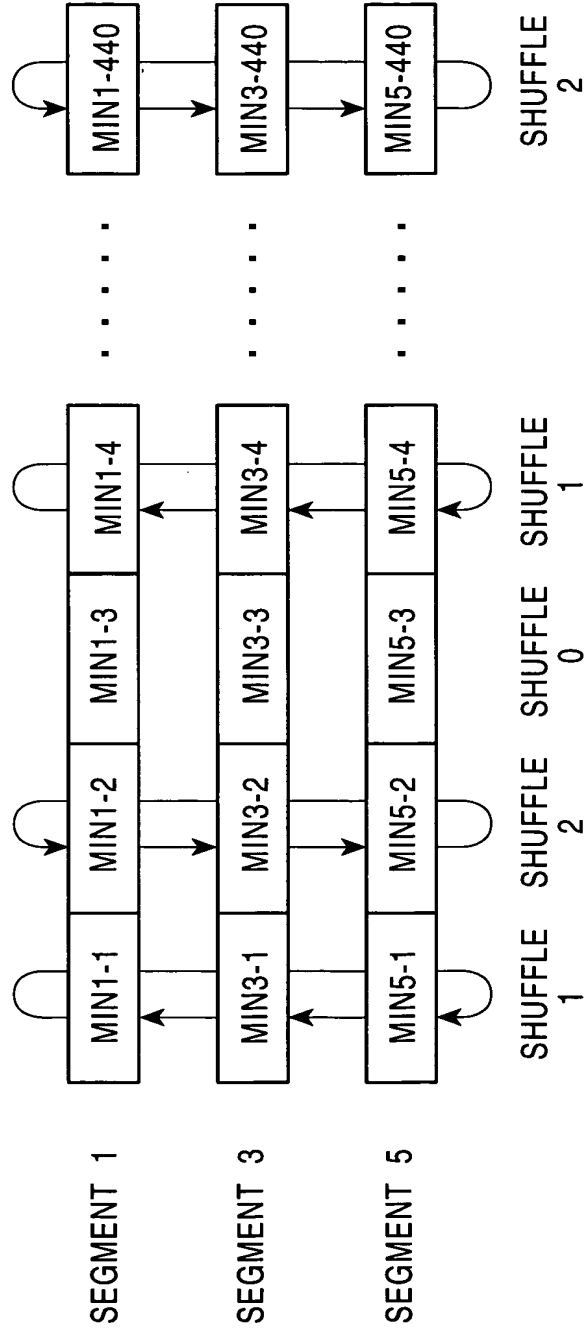


FIG. 25

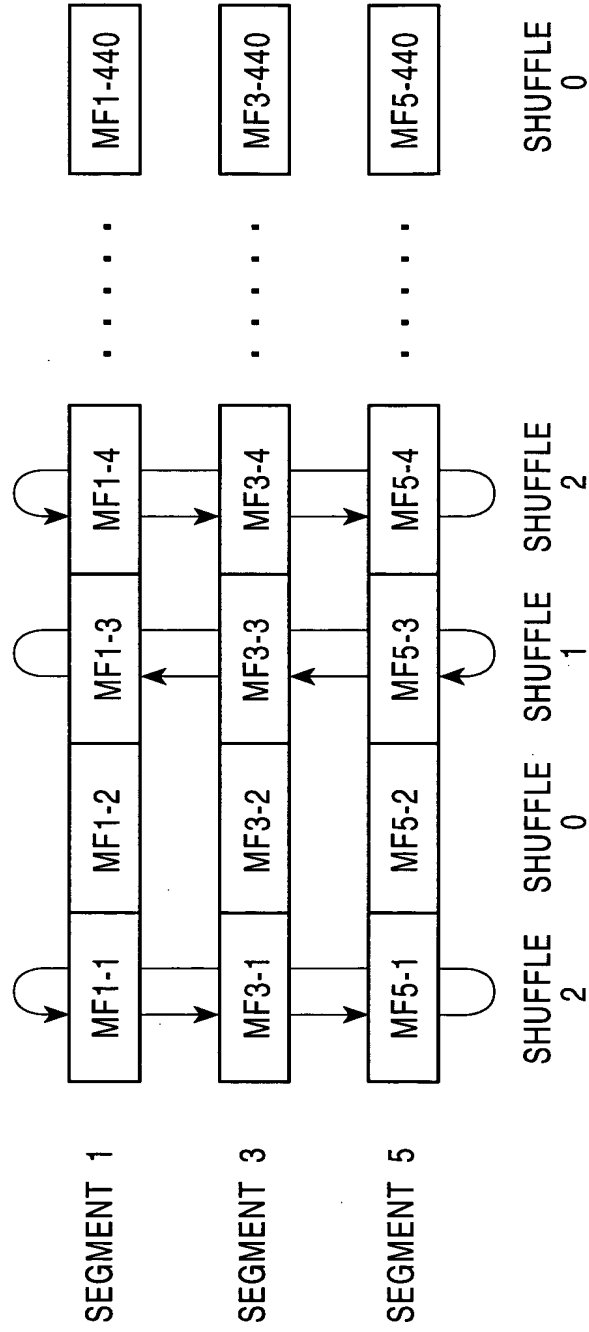


FIG. 26

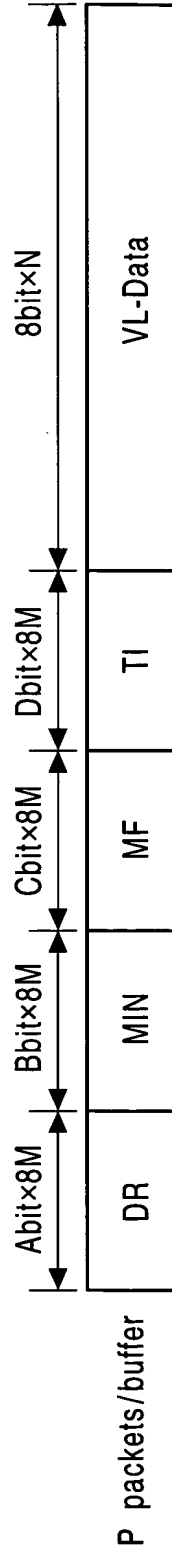


FIG. 27

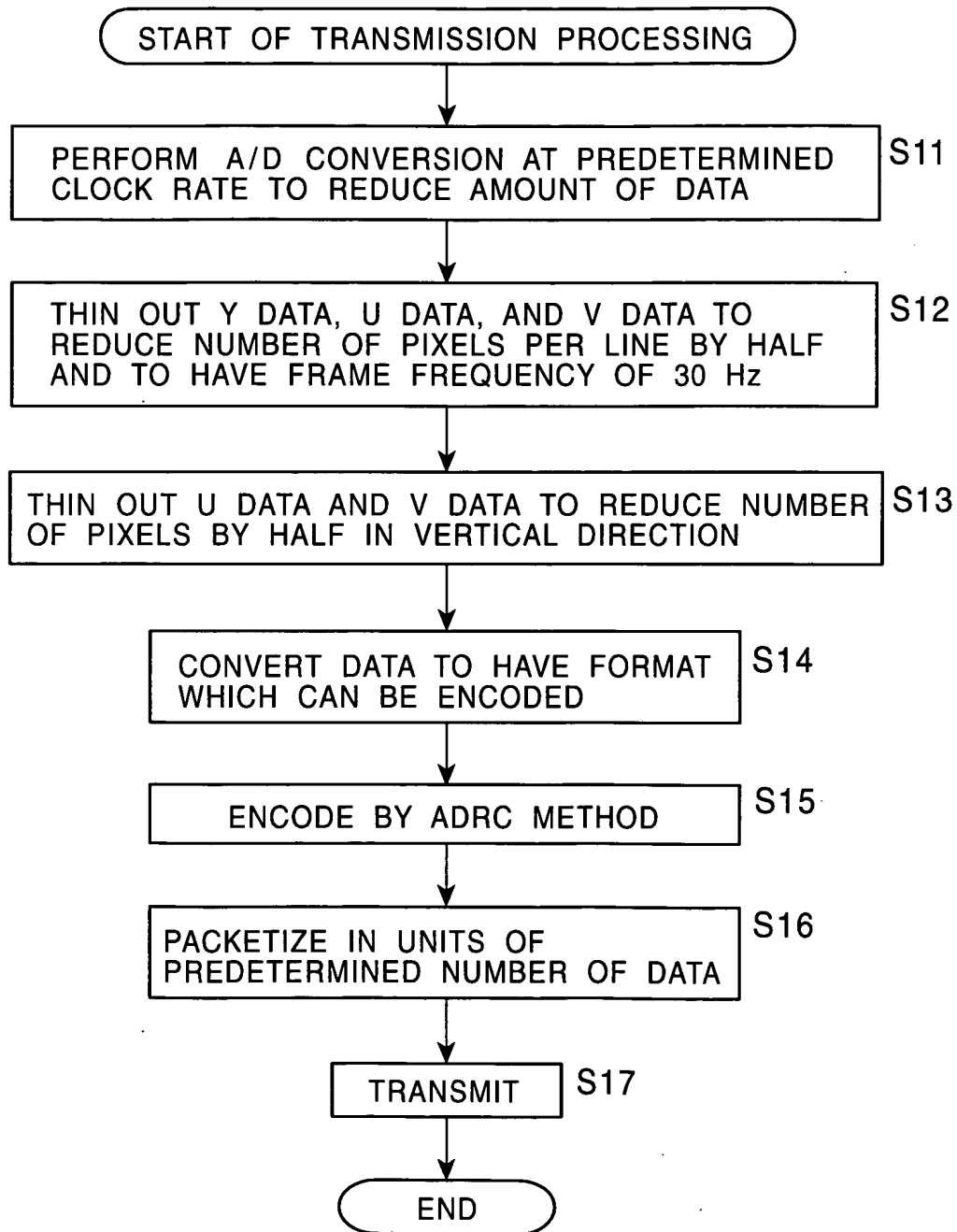


FIG. 28

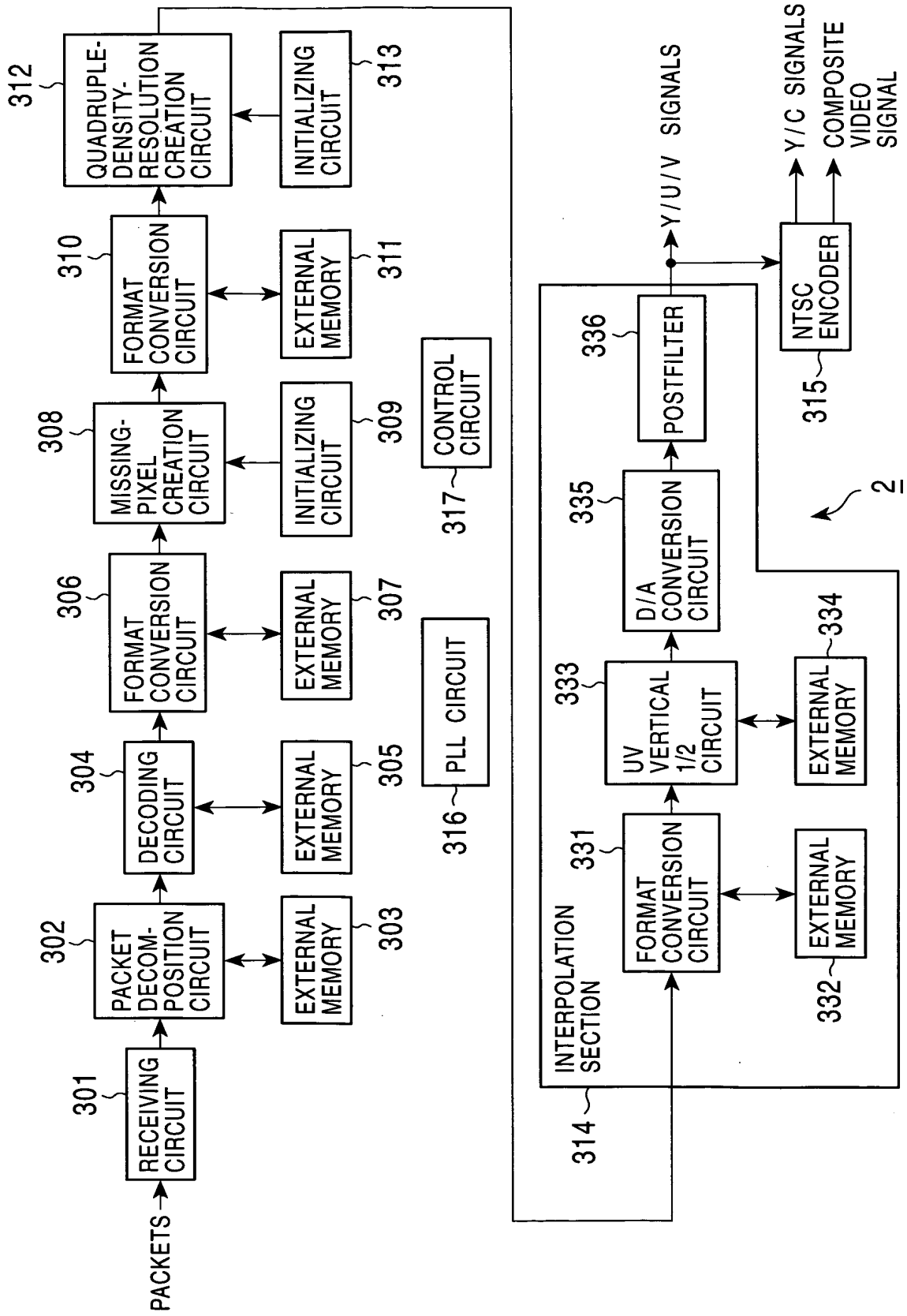


FIG. 29

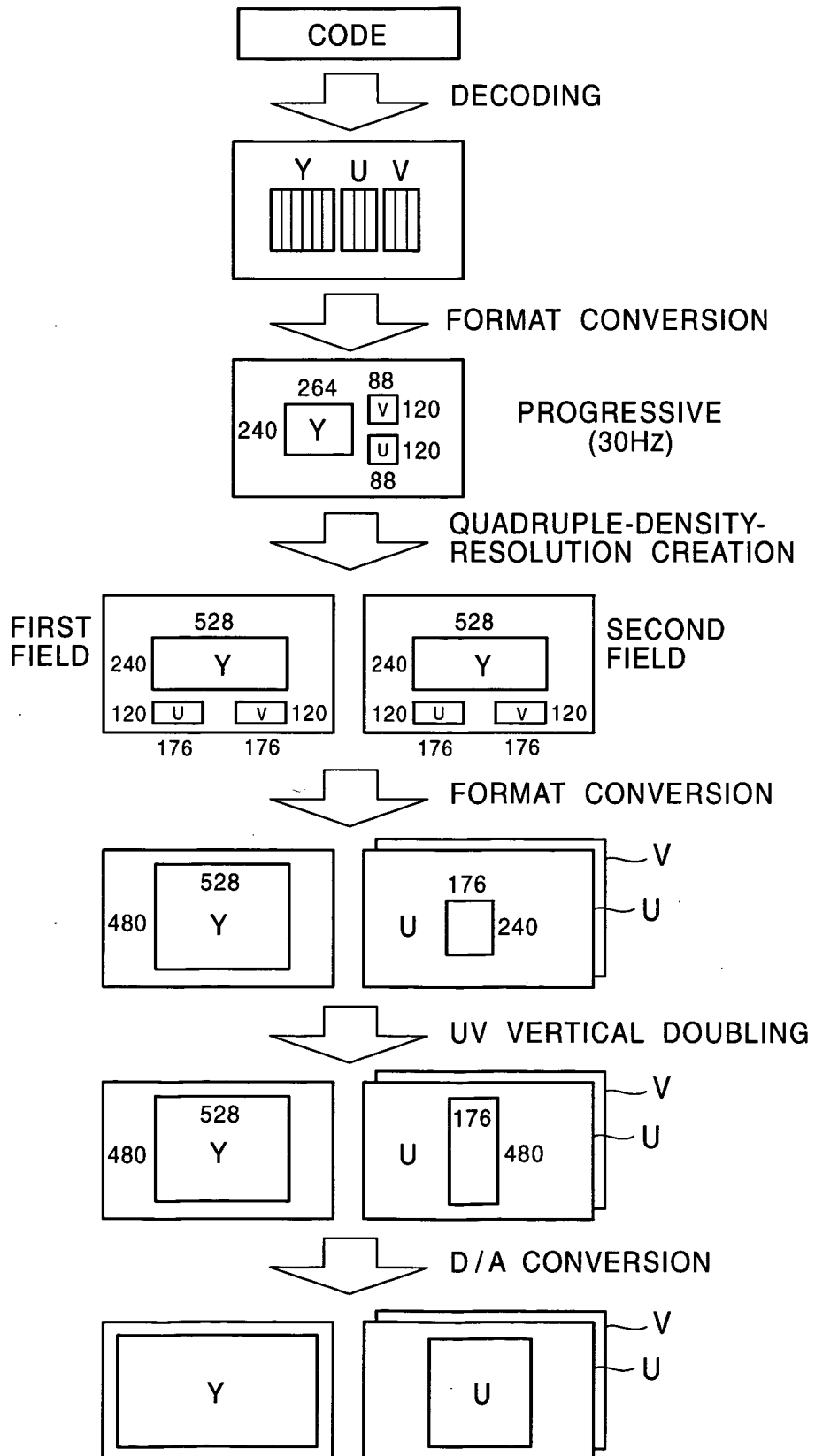


FIG. 30

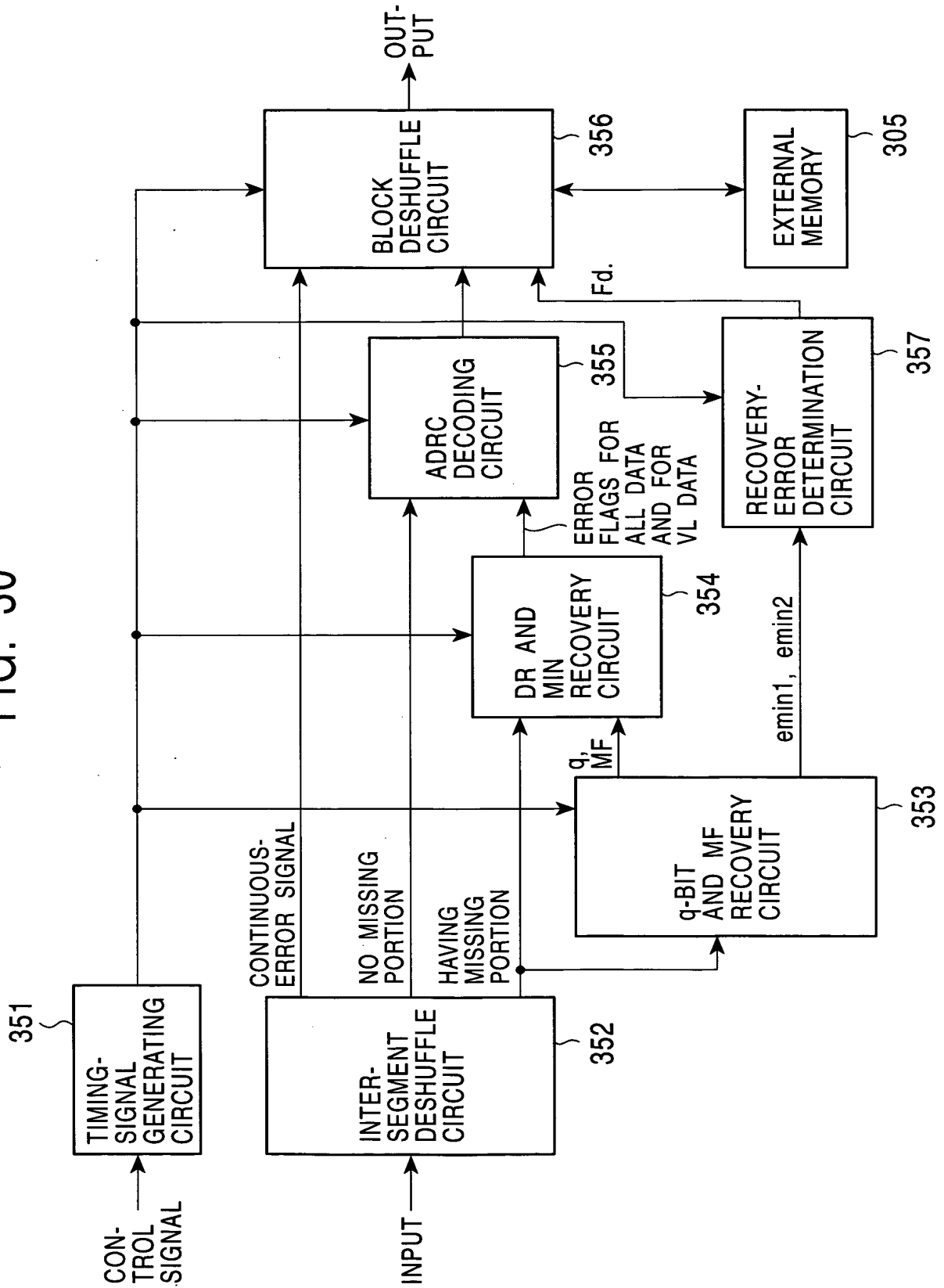


FIG. 31

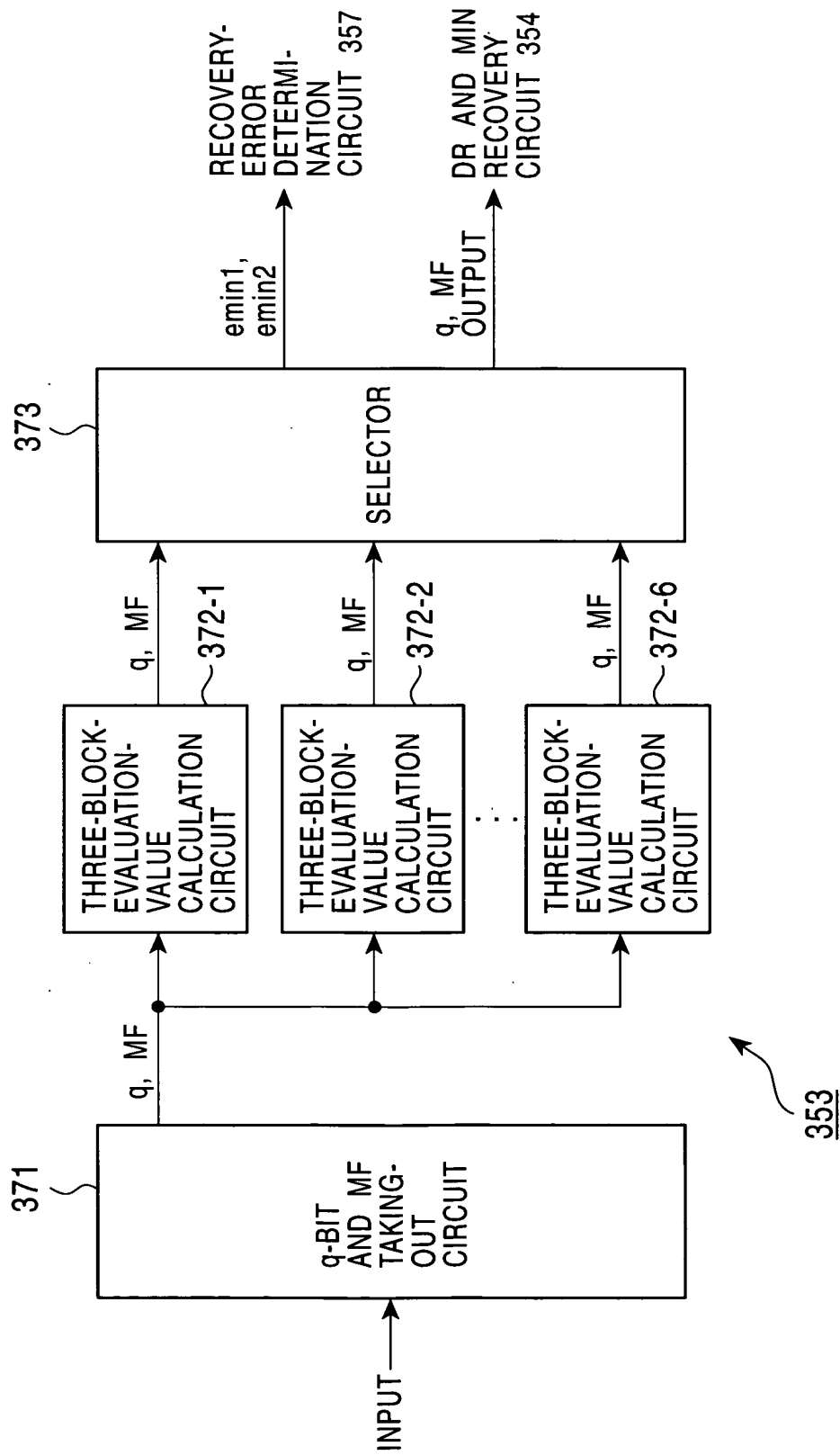


FIG. 32

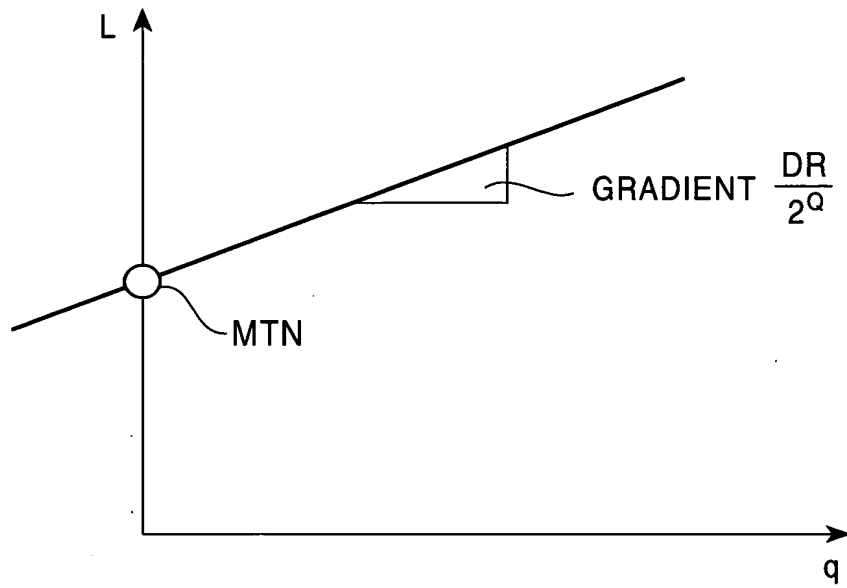


FIG. 33

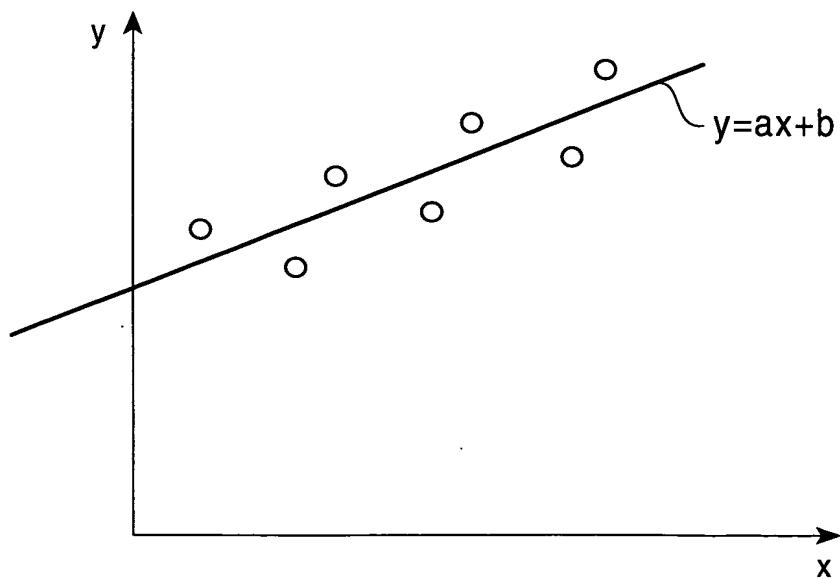


FIG. 34A

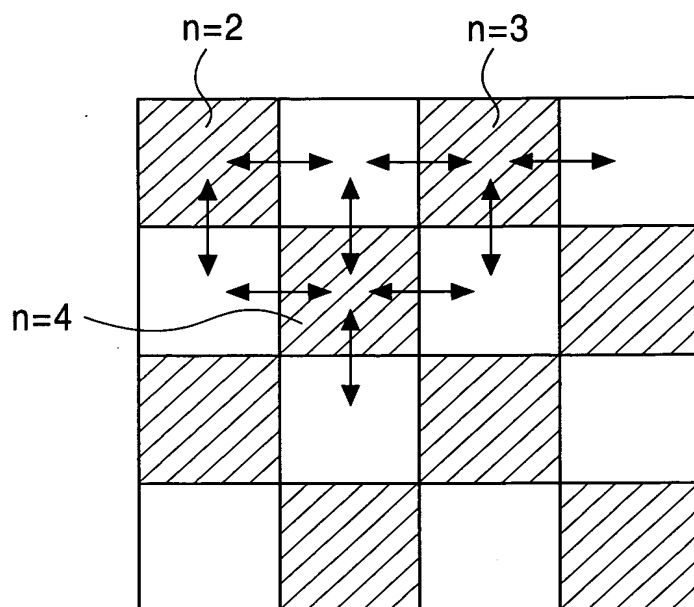


FIG. 34B

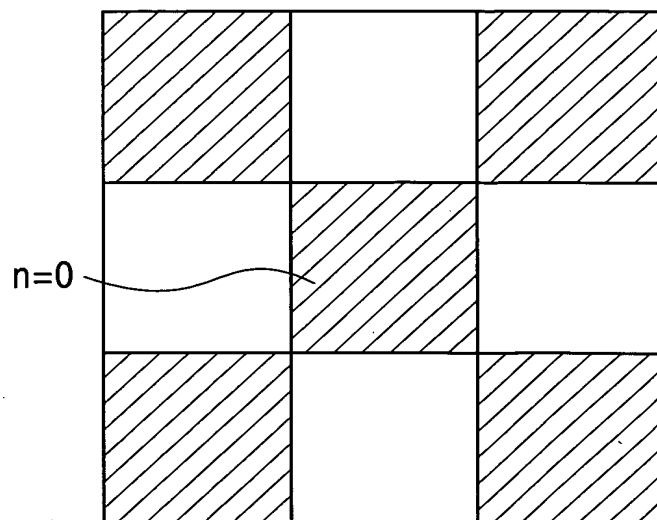


FIG. 35

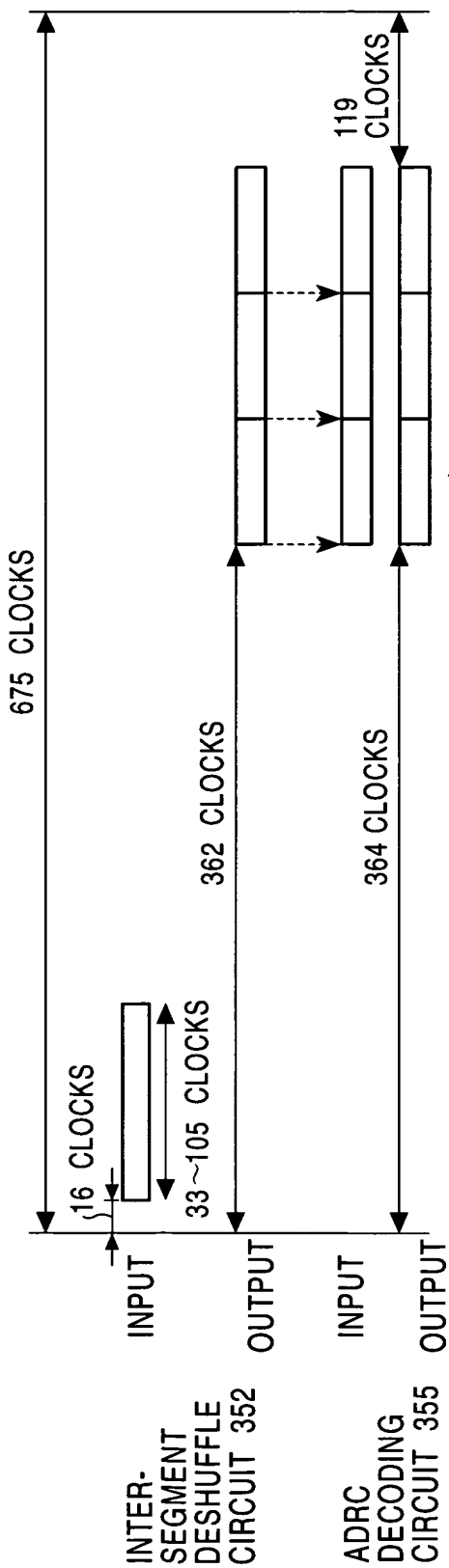


FIG. 36

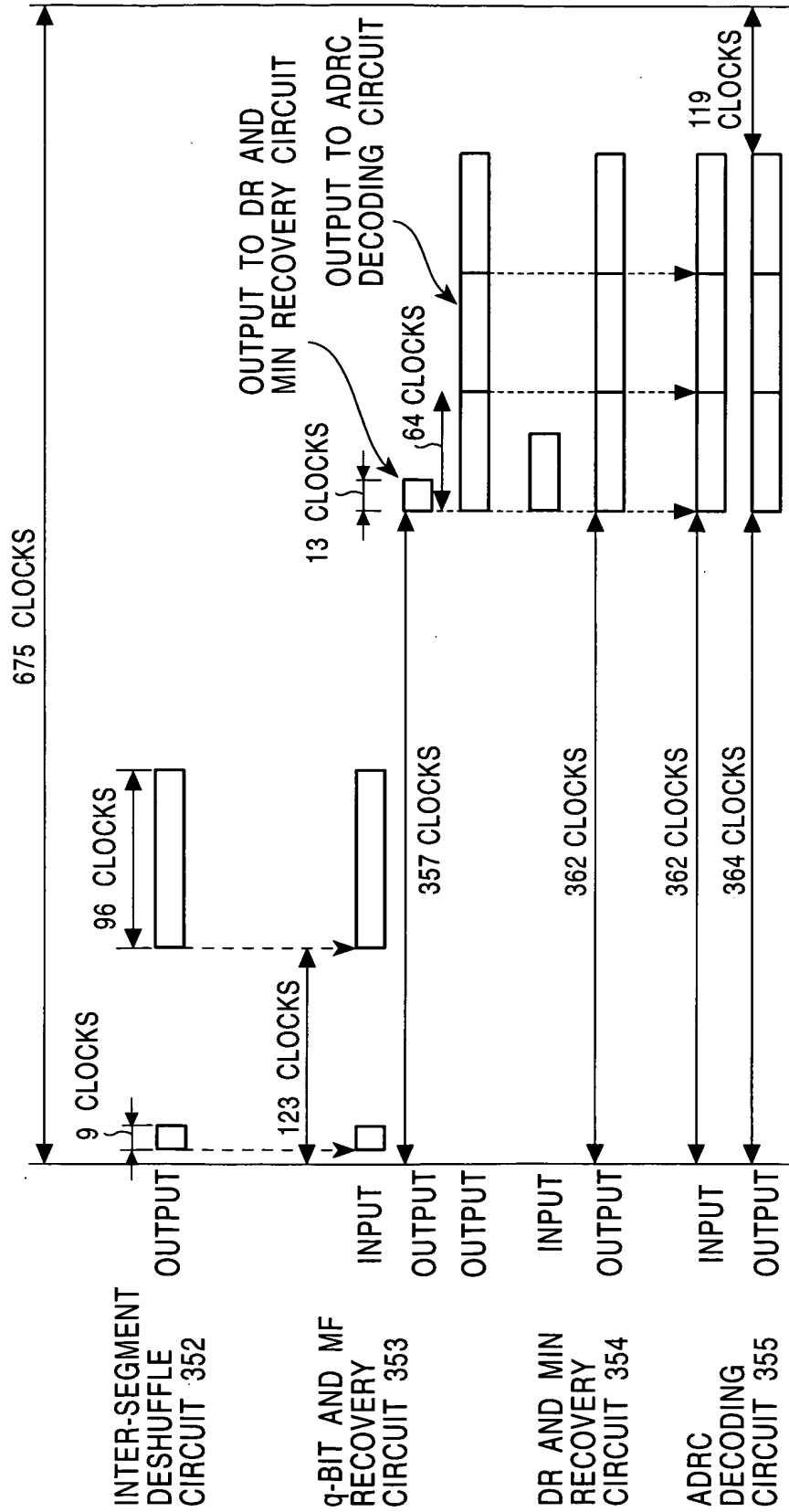


FIG. 37A

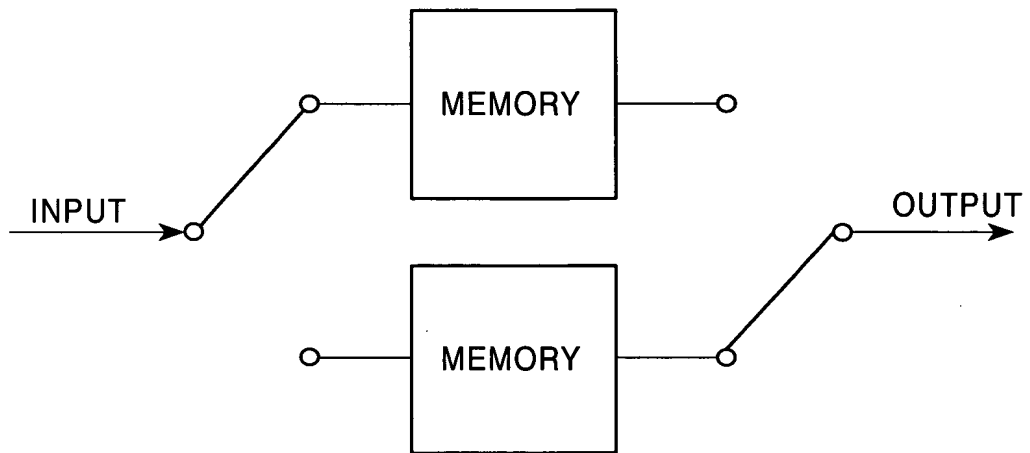


FIG. 37B

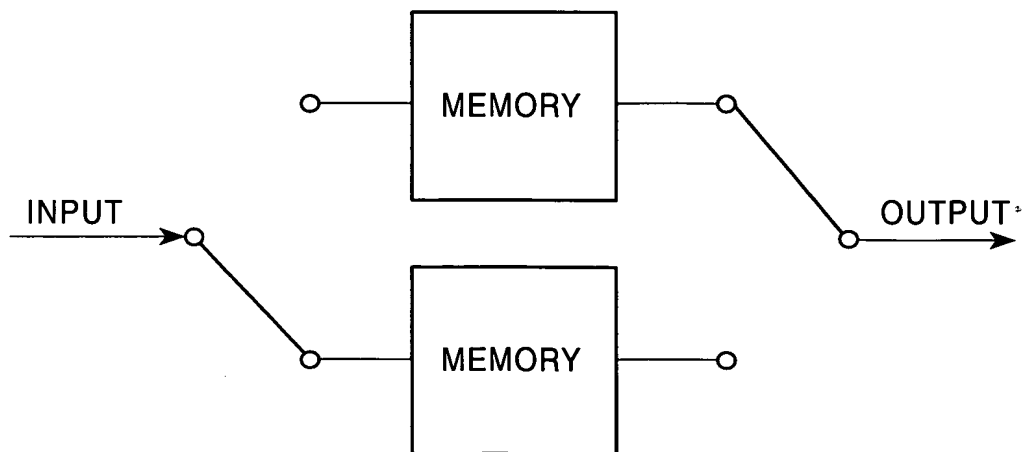


FIG. 38A

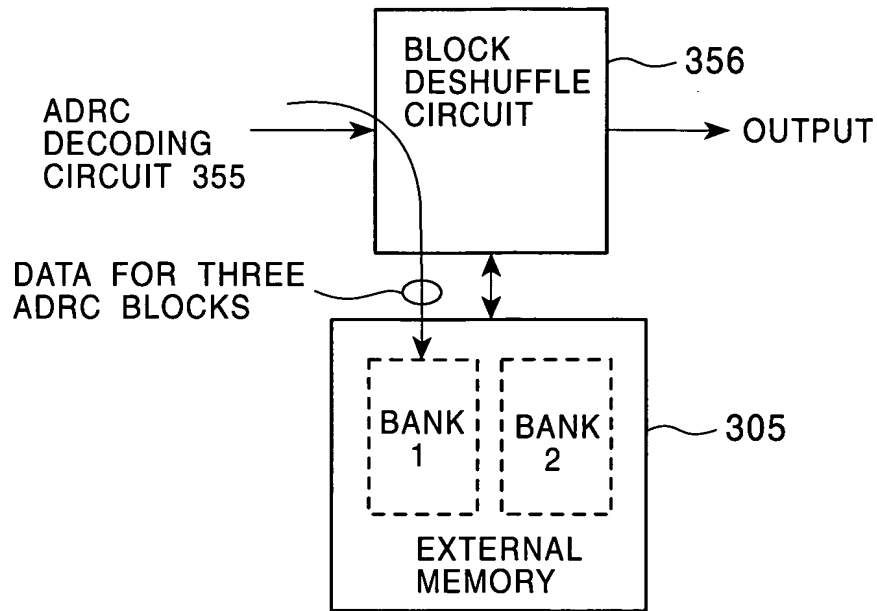


FIG. 38B

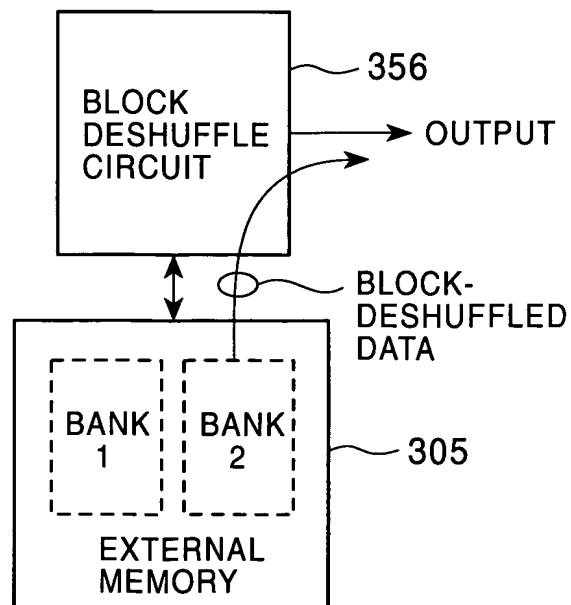


FIG. 39

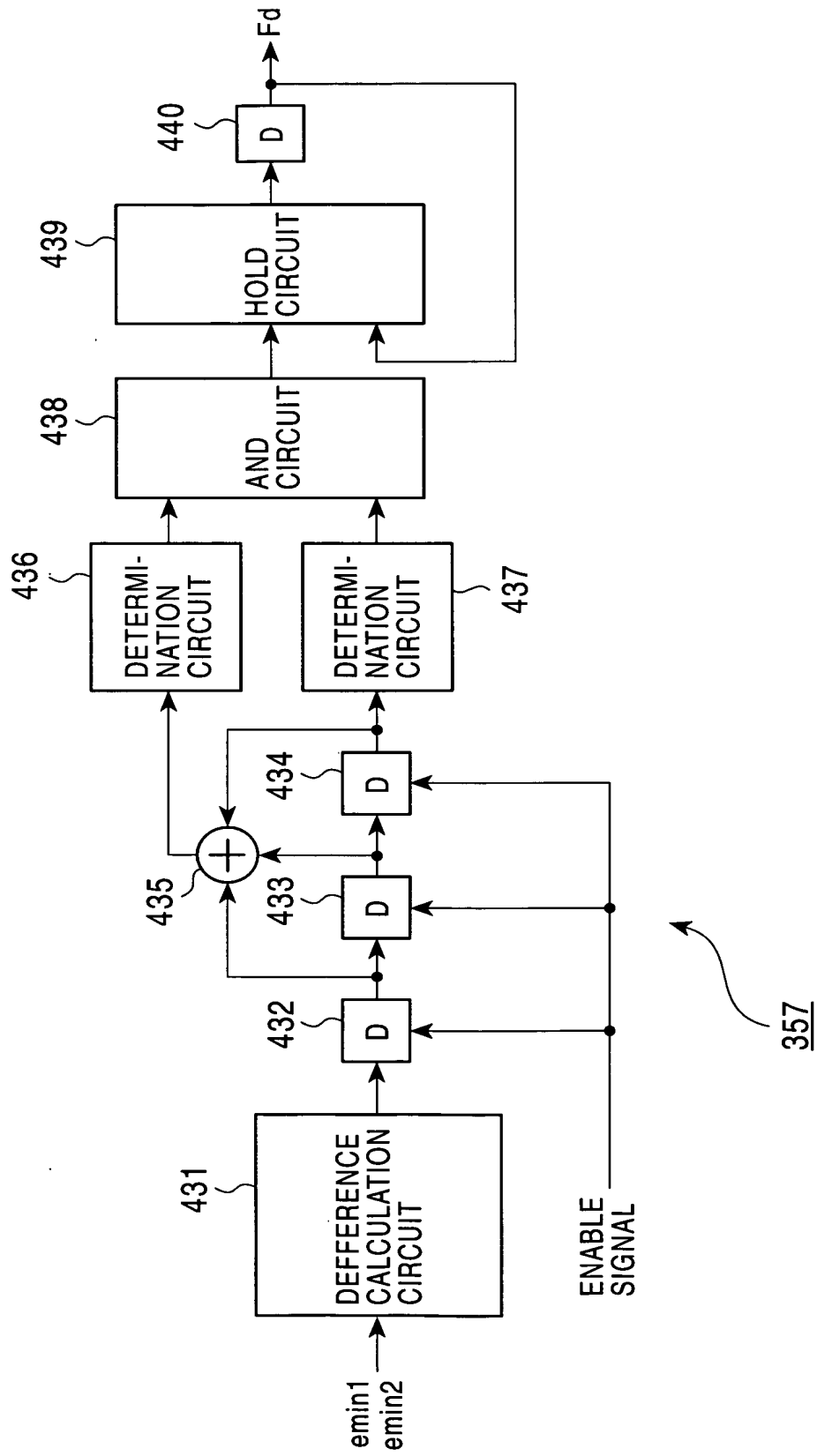


FIG. 40

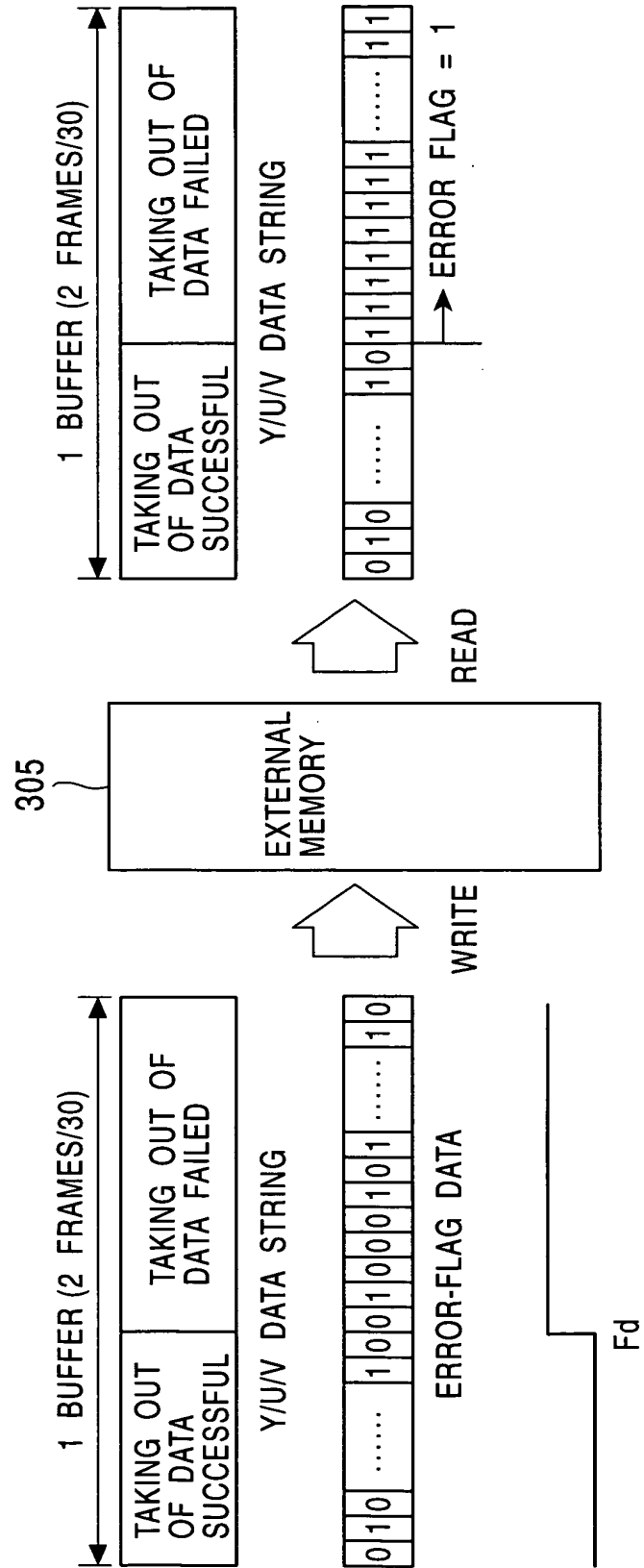


FIG. 41

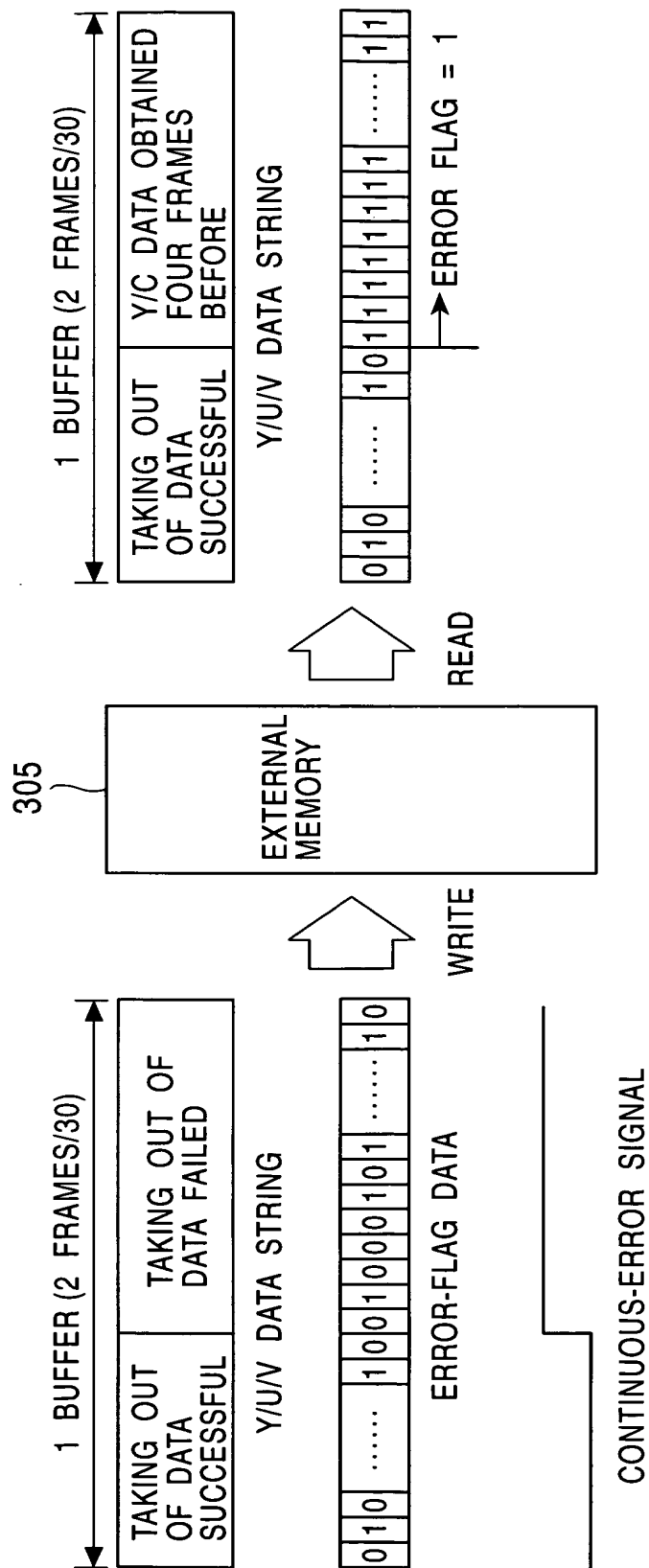


FIG. 43

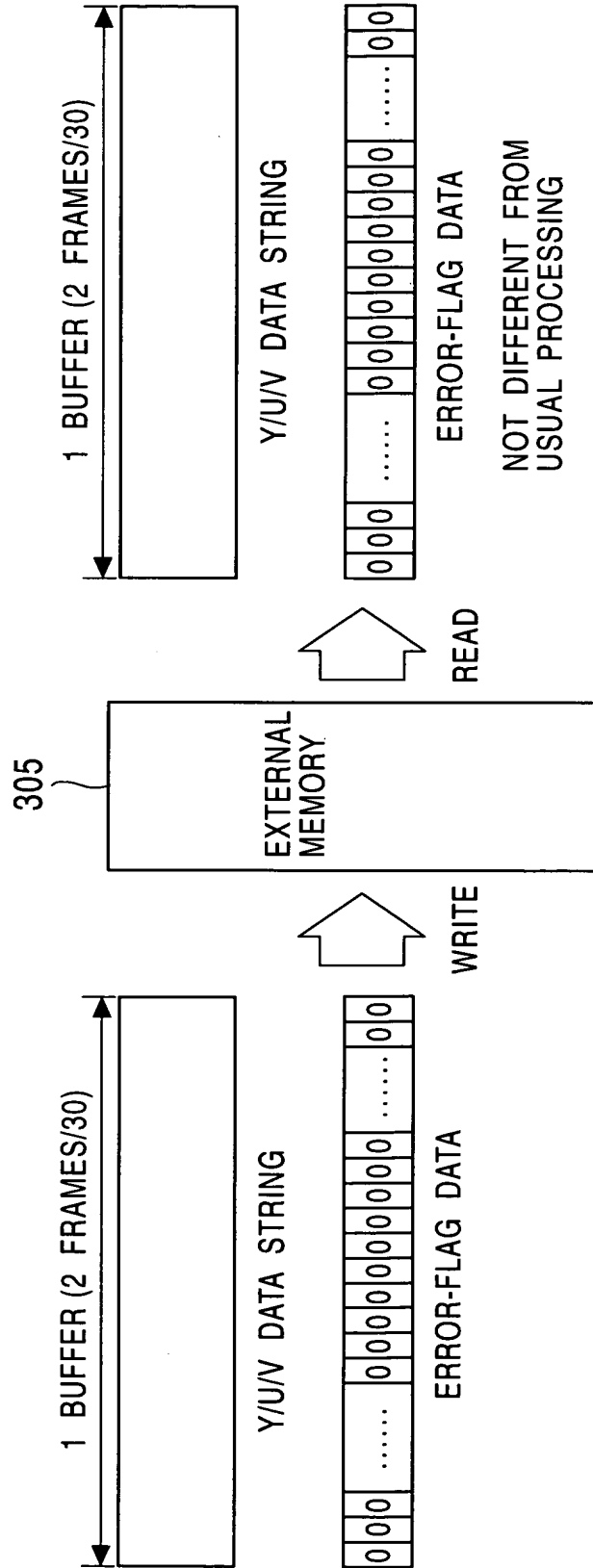


FIG. 44

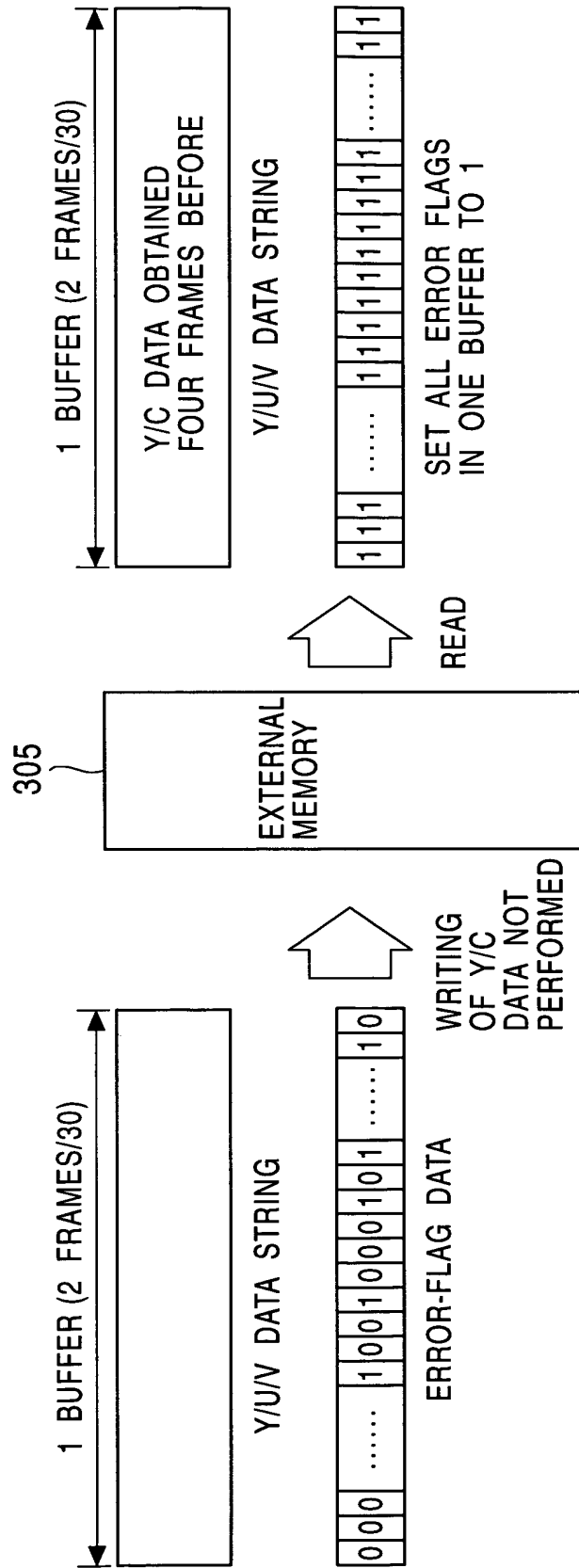


FIG. 46

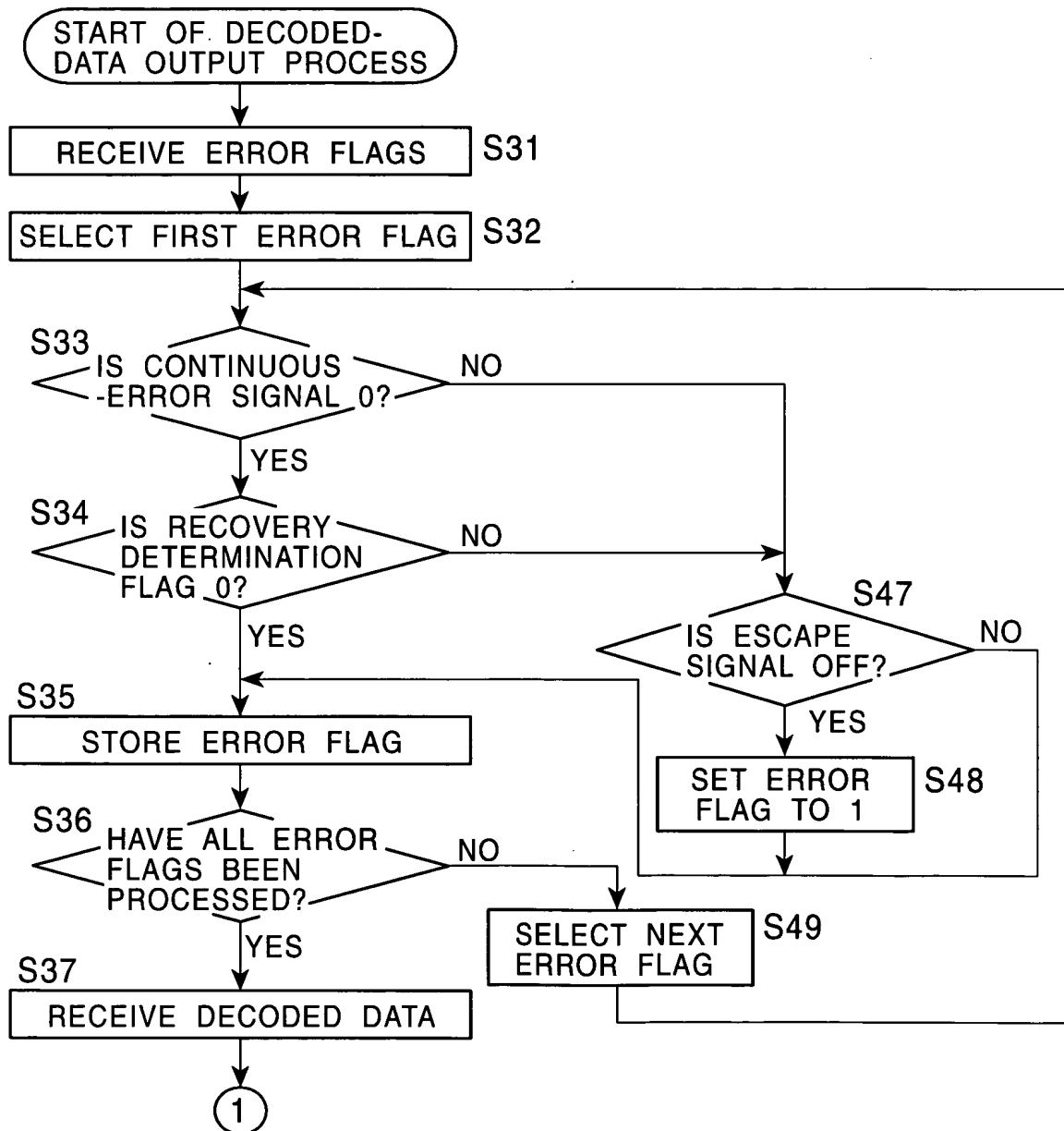


FIG. 47

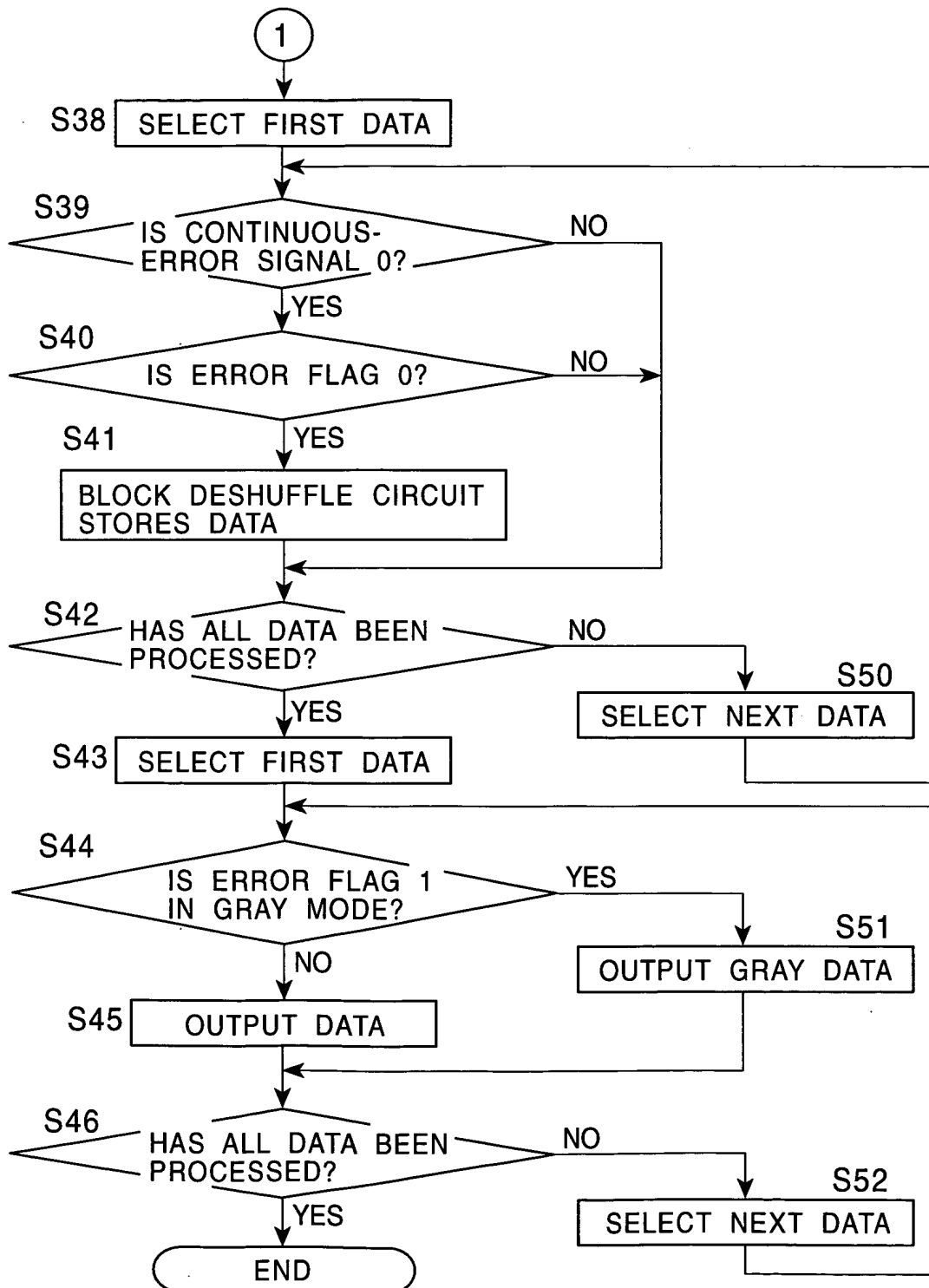


FIG. 48

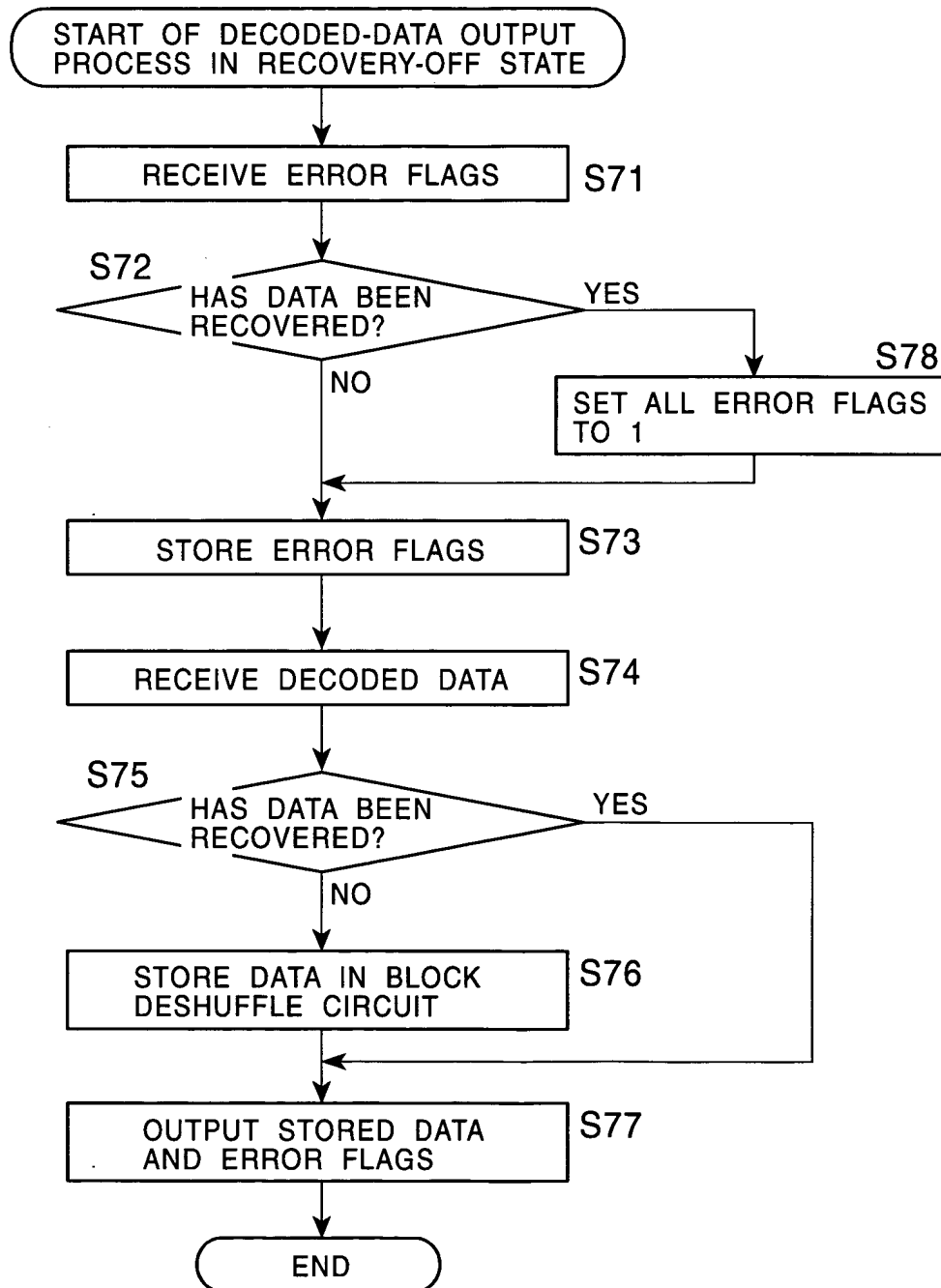


FIG. 49A

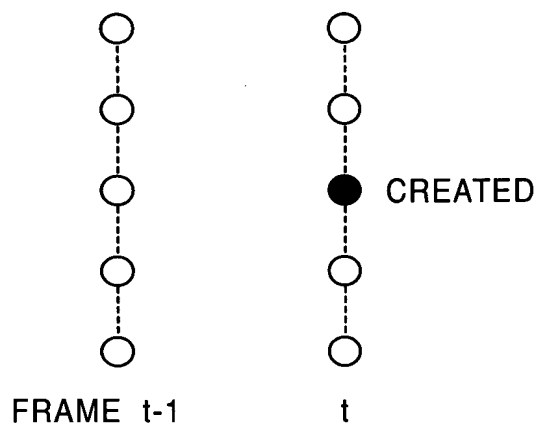


FIG. 49B

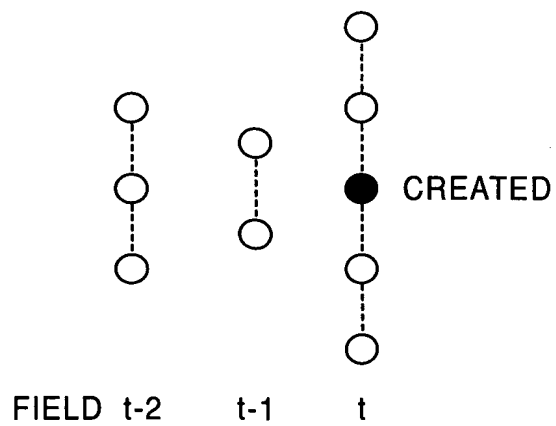


FIG. 50

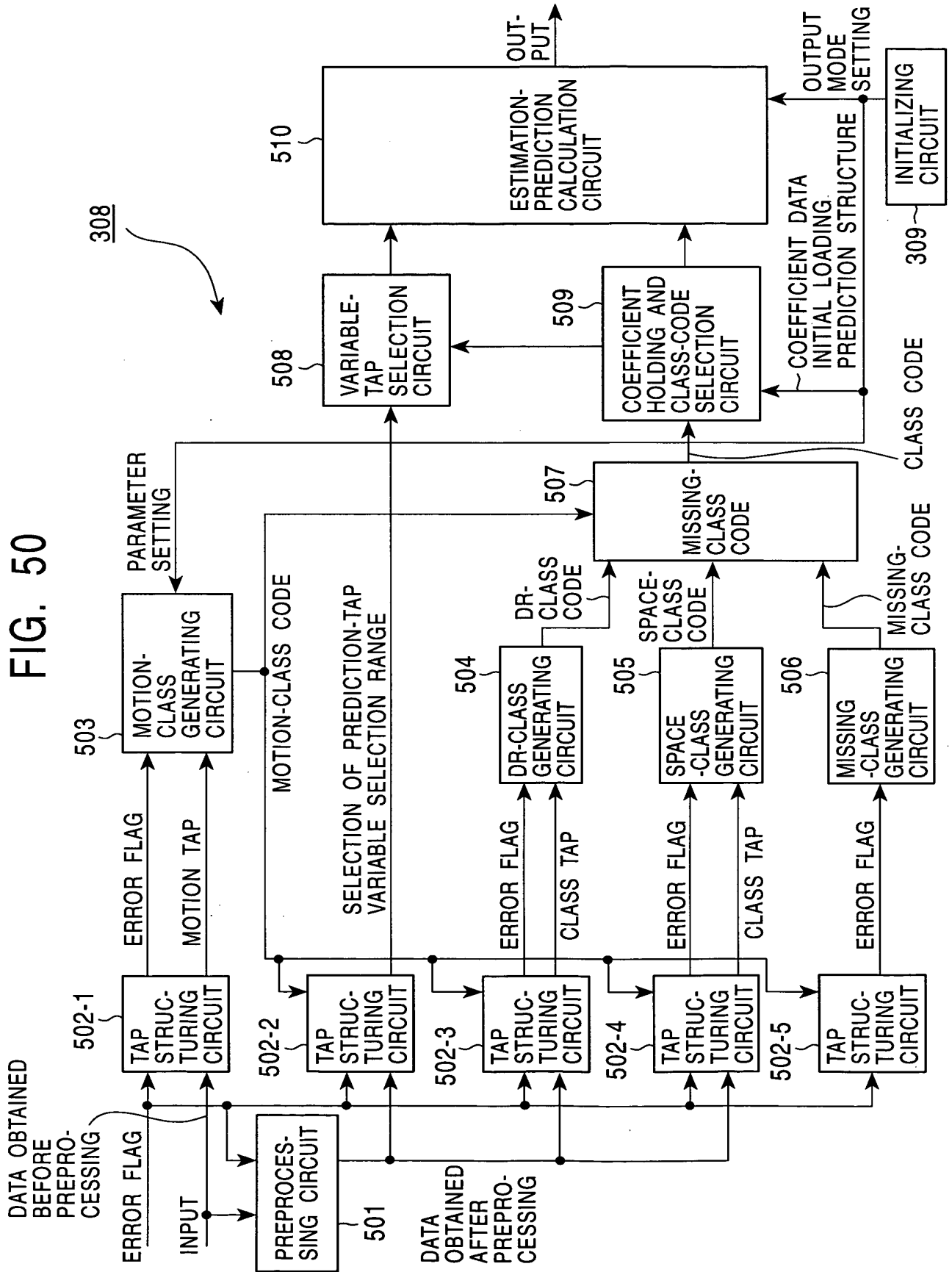


FIG. 51

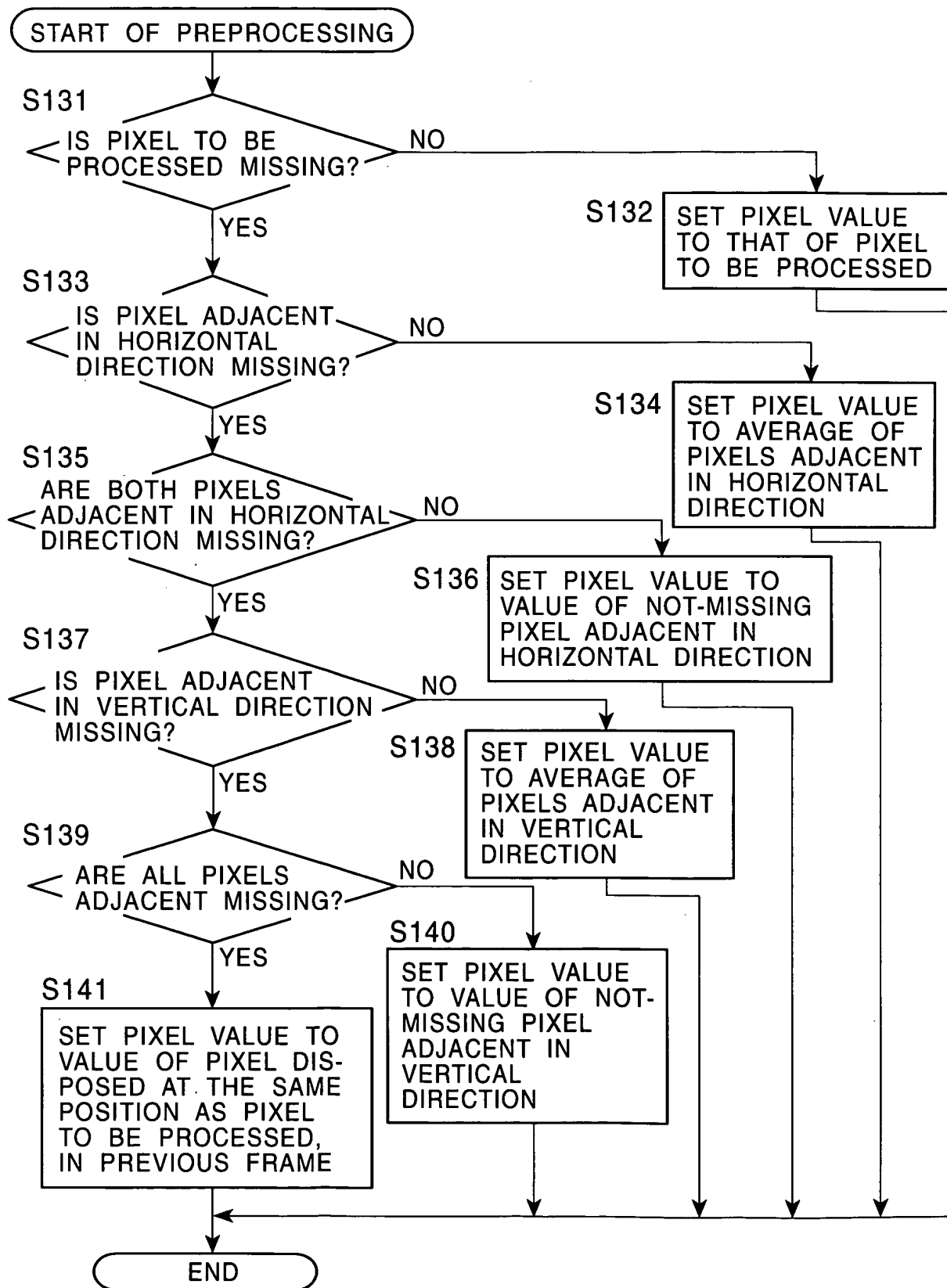


FIG. 52A

	H1	H2	H3
L1	ERROR	q2	q3
L2	q4	ERROR	q6
L3	q7	ERROR	q9

FRAME t

FIG. 52B

	H1	H2	H3
L1	p1	p2	p3
L2	p4	p5	p6
L3	p7	p8	p9

FRAME t-1

FIG. 53

q1	q2	q3
q4	ERROR	q6
q7	q8	q9

FRAME t

FIG. 52A

FIG. 54

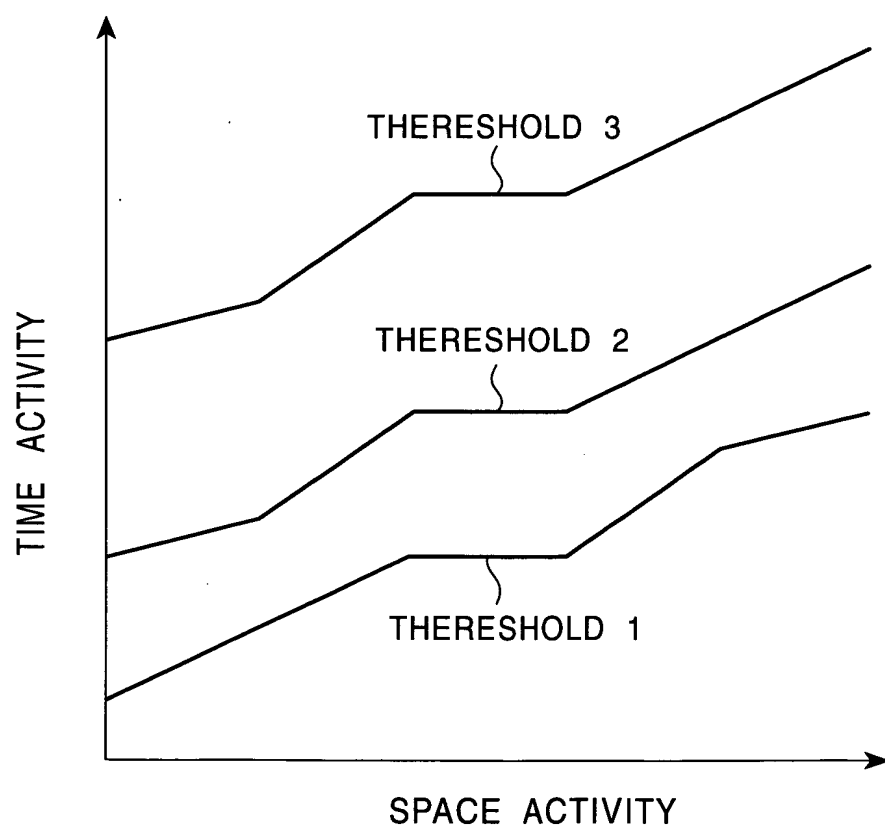


FIG. 55

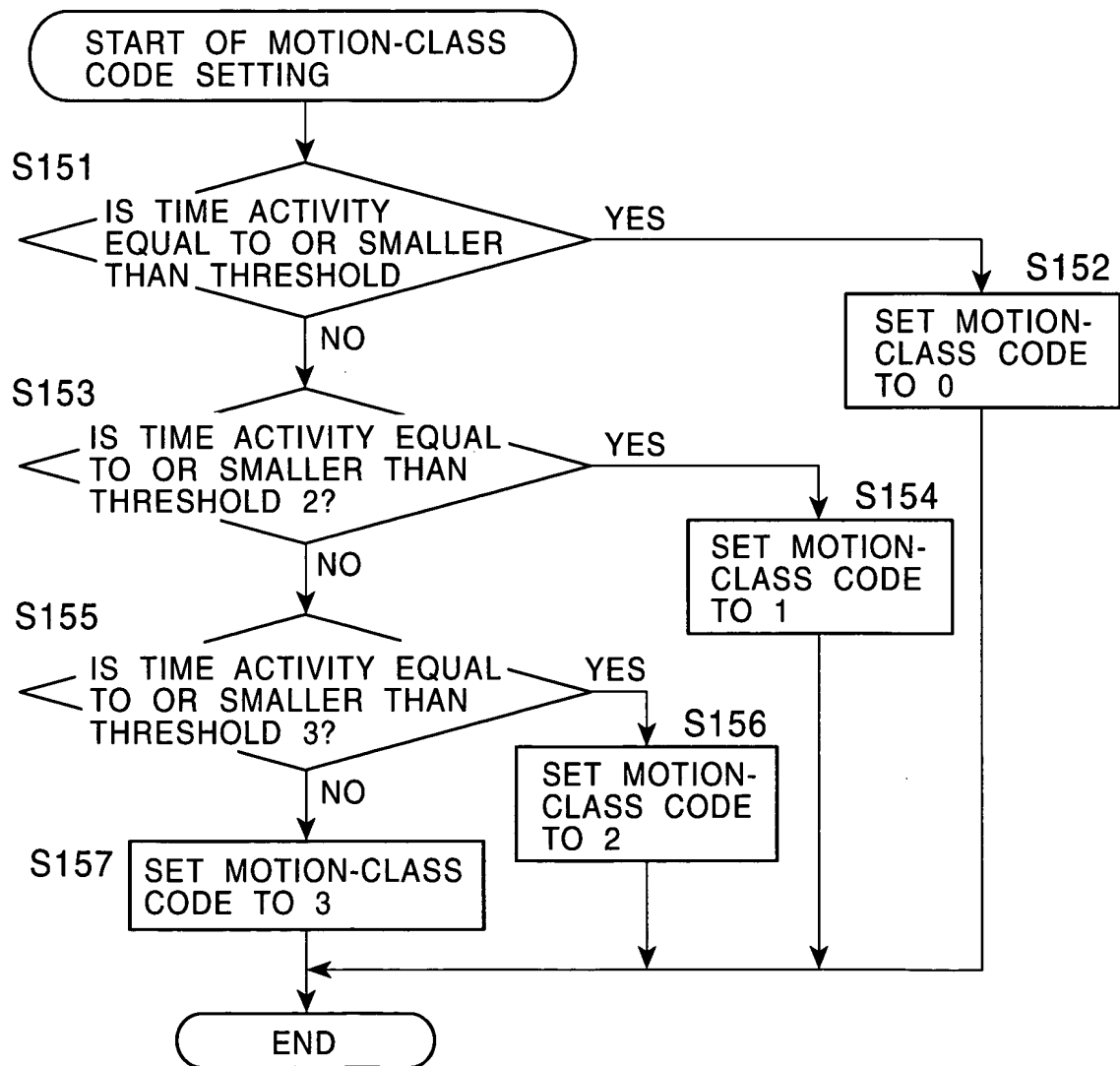
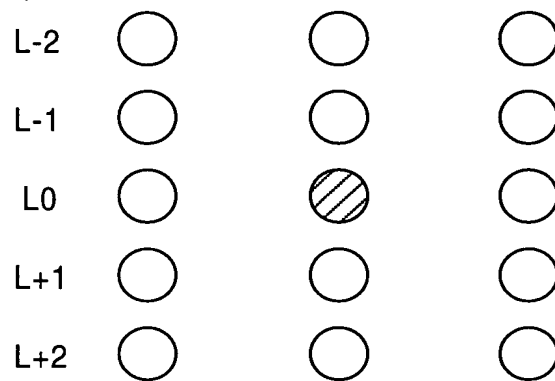


FIG. 56




 : PIXEL TO BE PROCESSED

FIG. 57

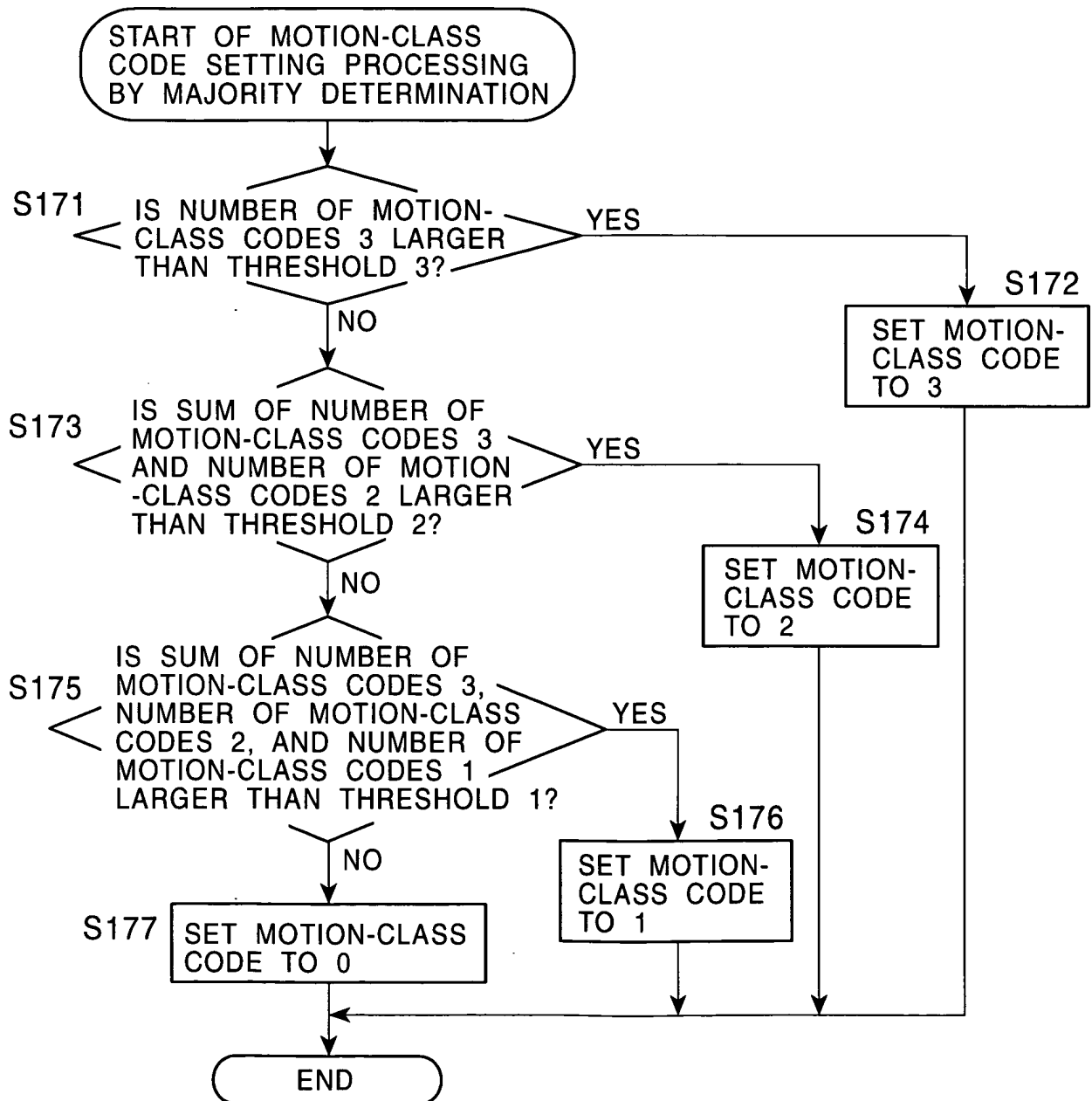


FIG. 58

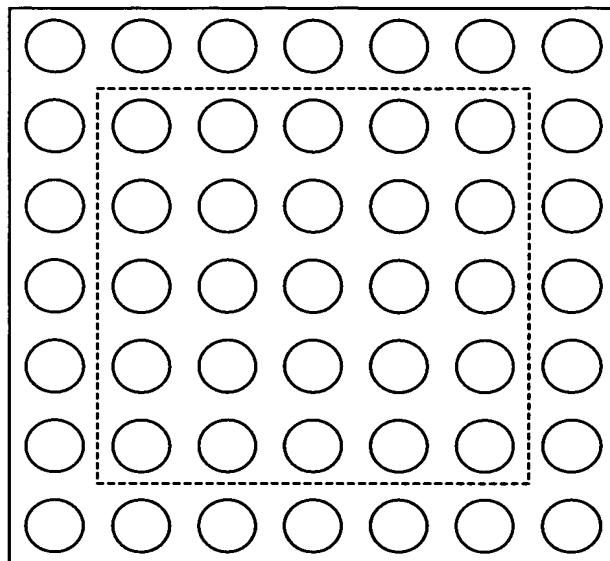


FIG. 59

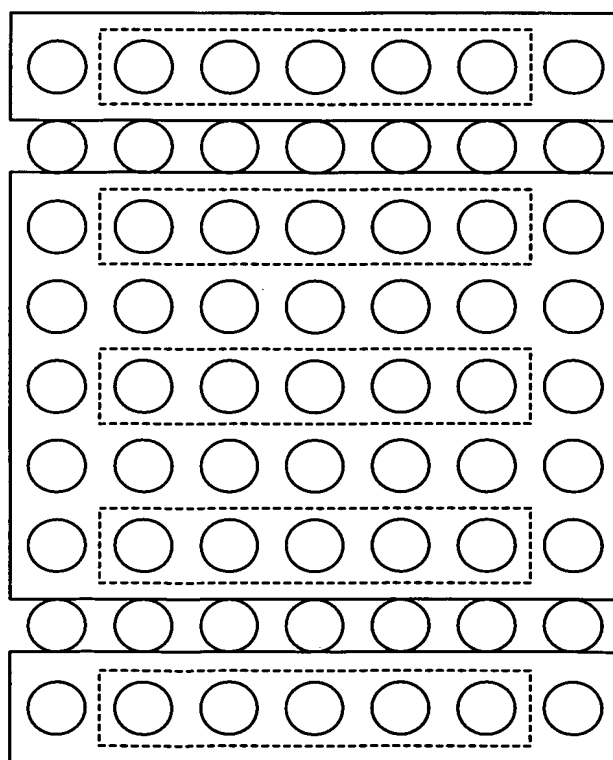


FIG. 60

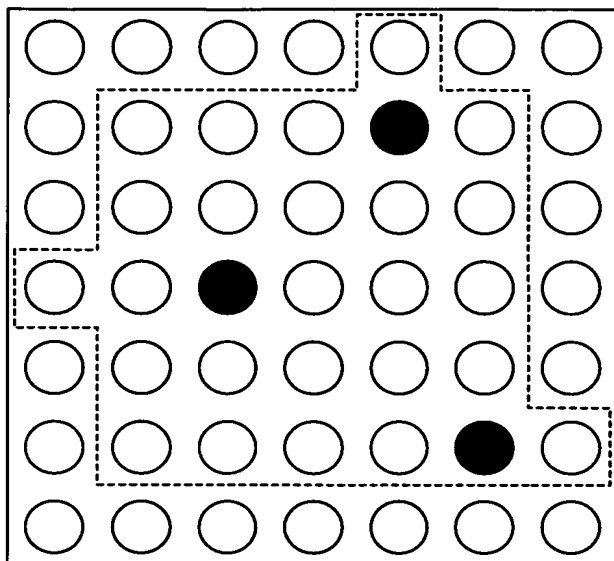


FIG. 61

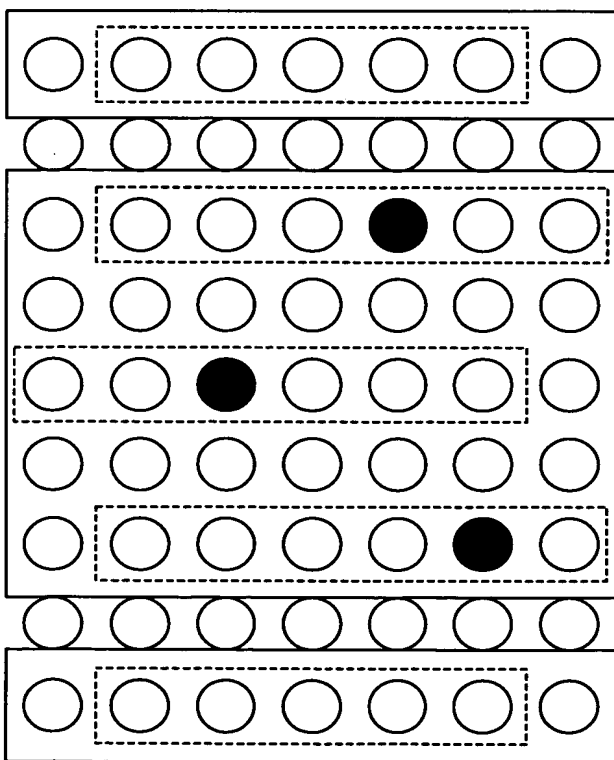


FIG. 62A

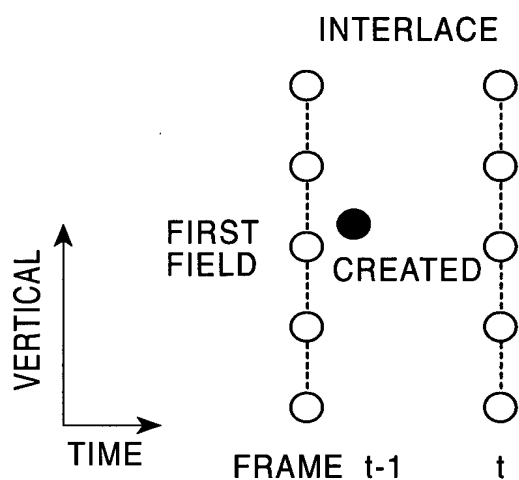


FIG. 62C

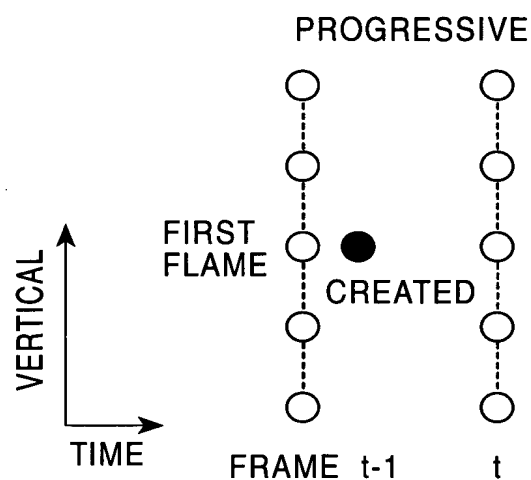


FIG. 62B

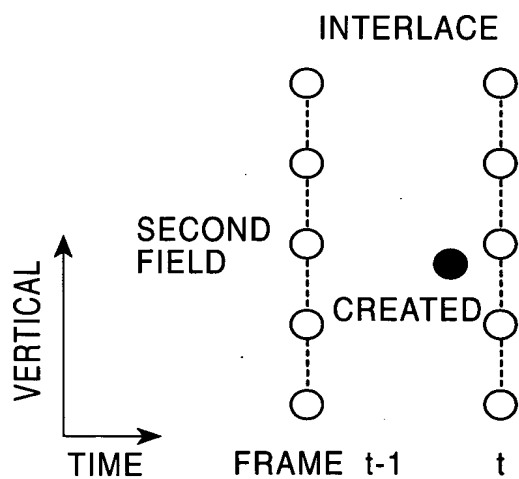


FIG. 62D

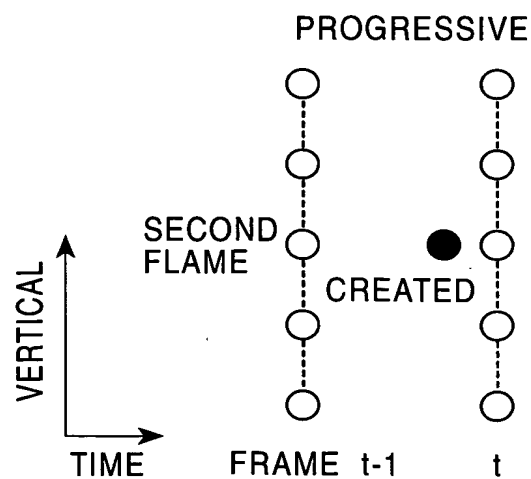


FIG. 63

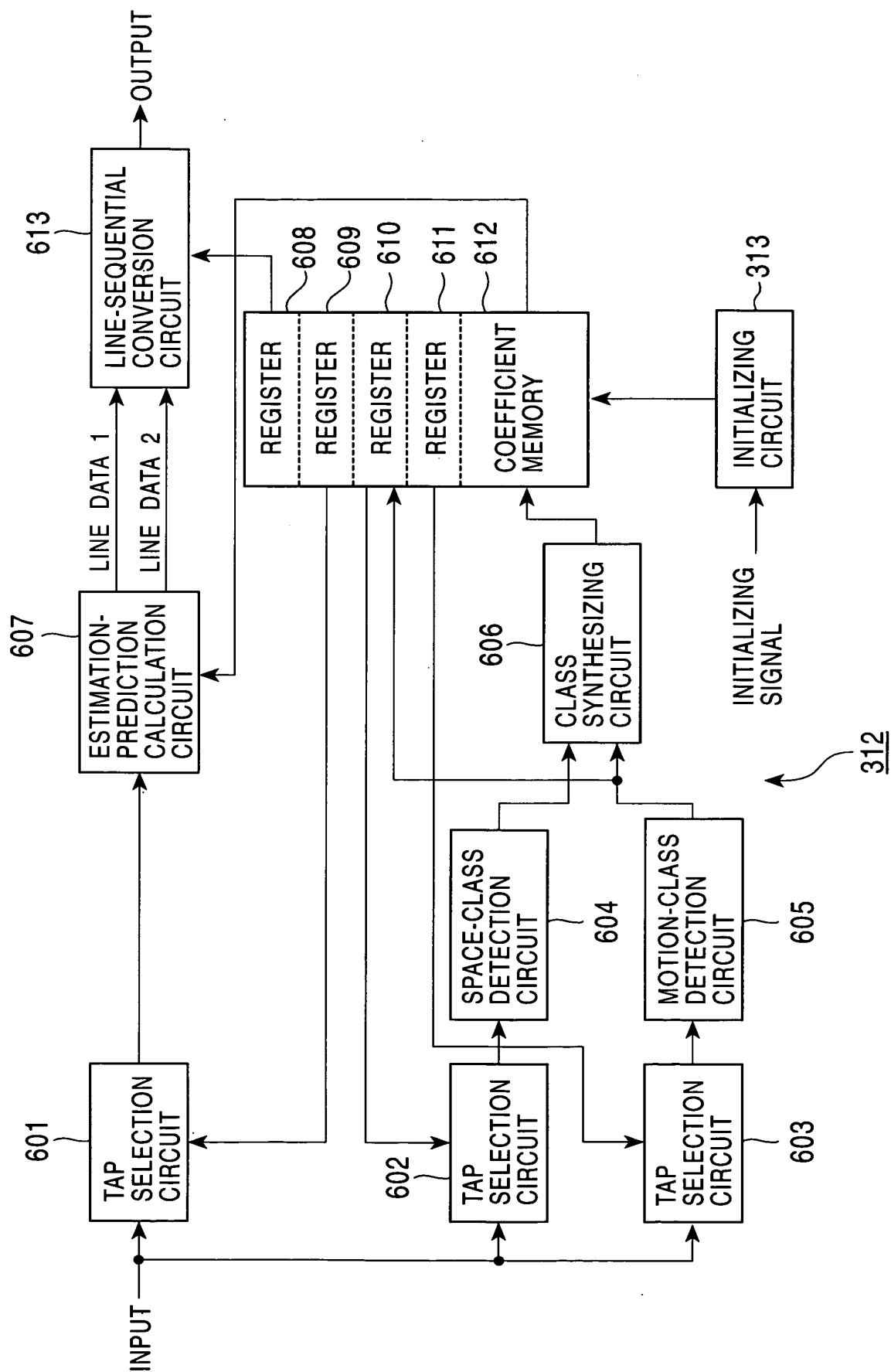


FIG. 64

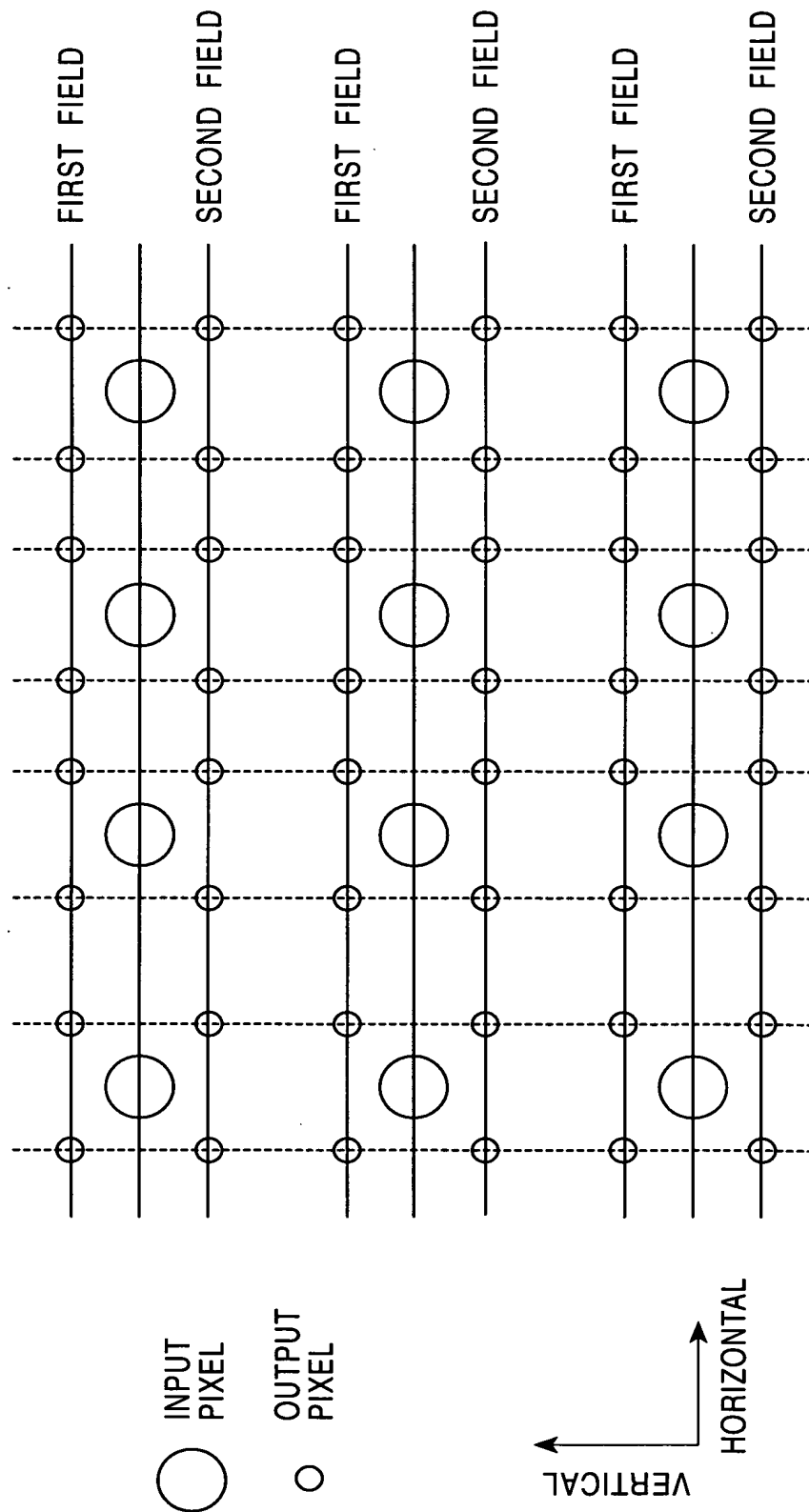


FIG. 65

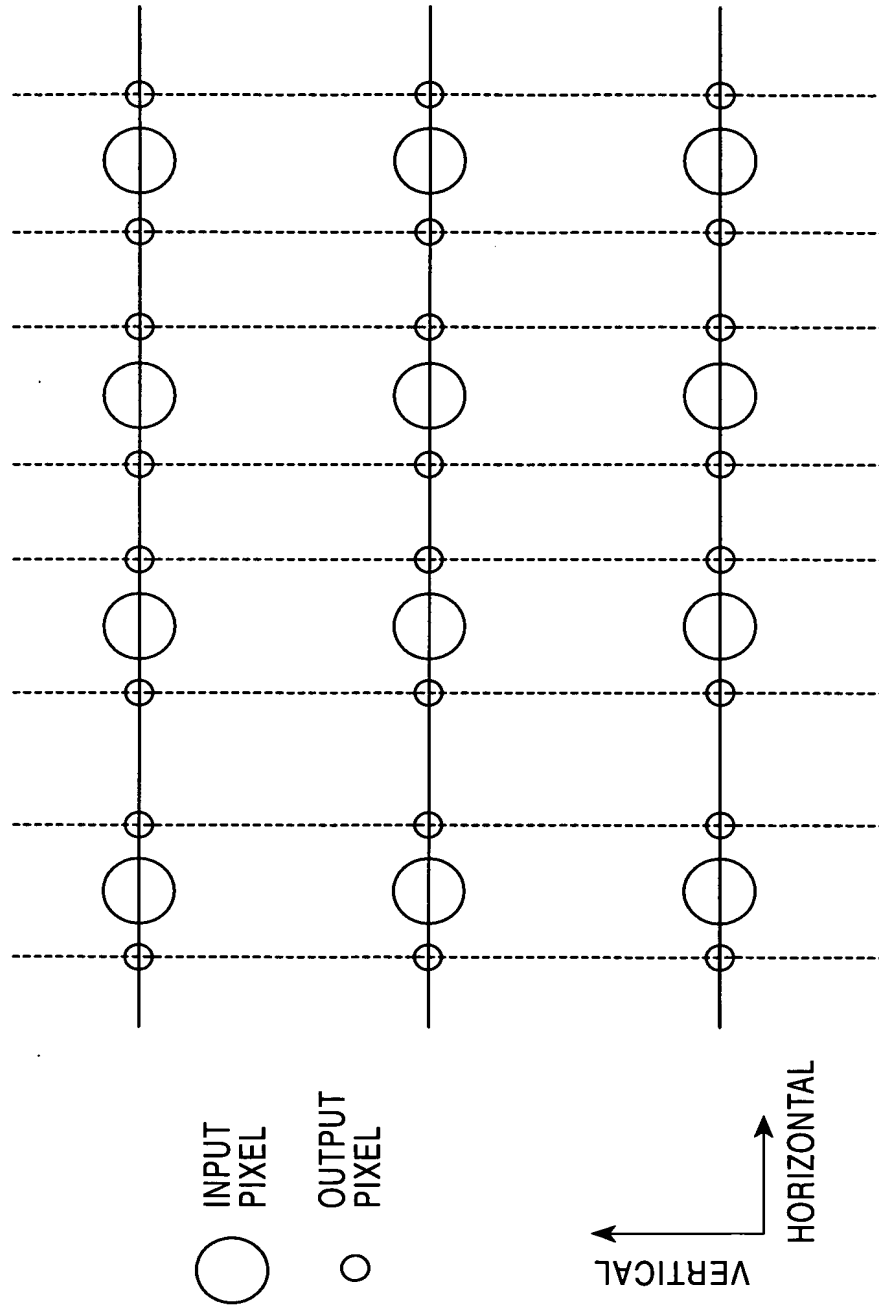


FIG. 66

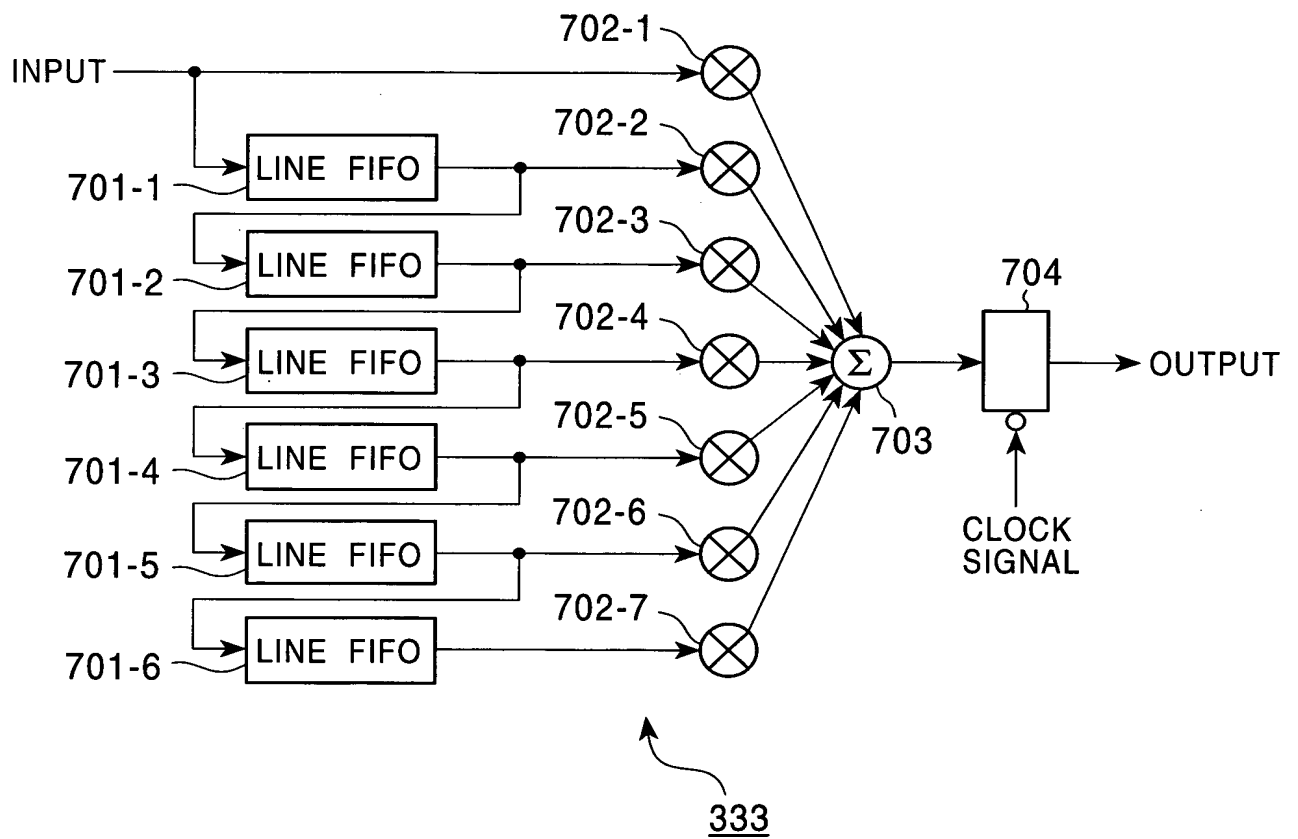


FIG. 67

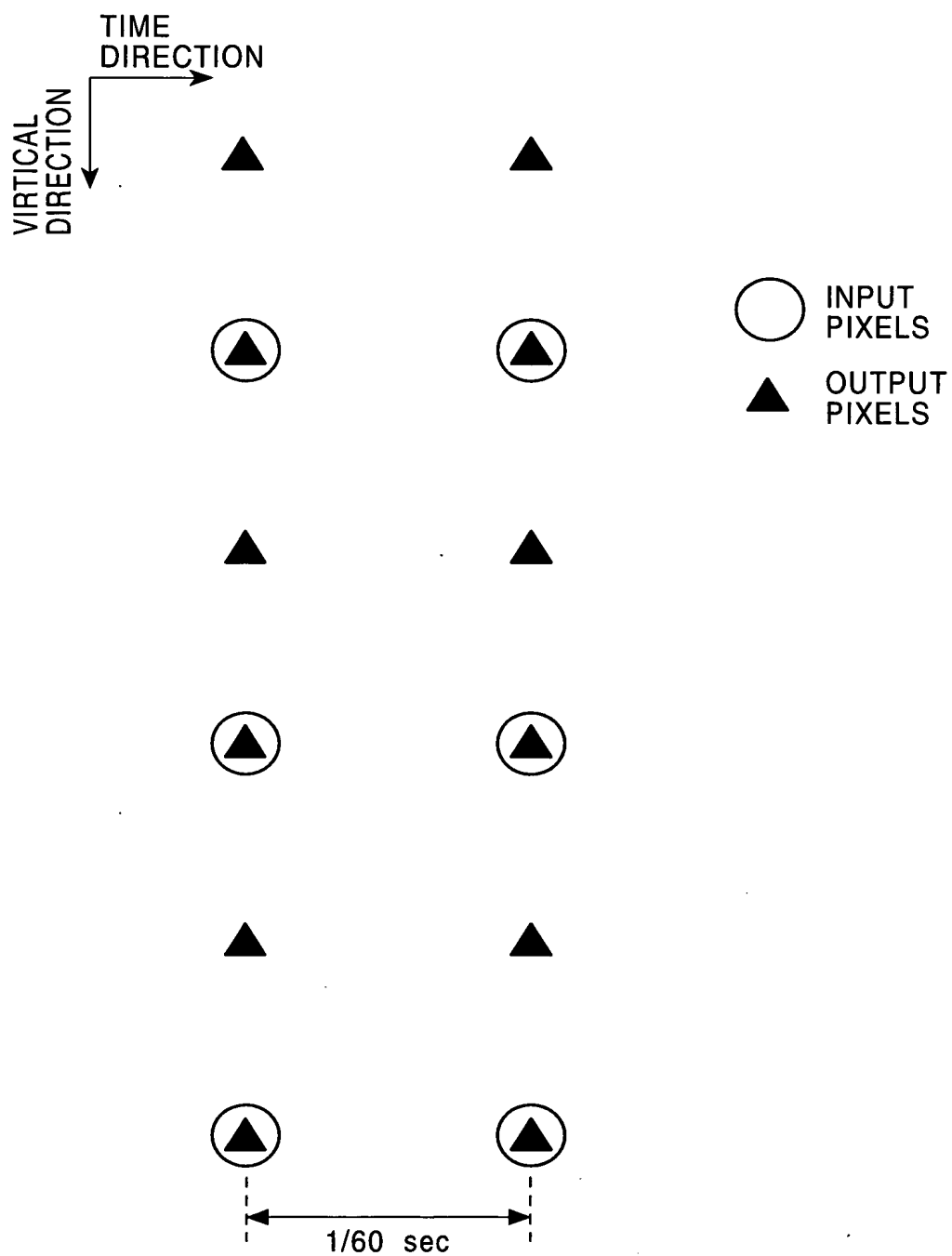


FIG. 68

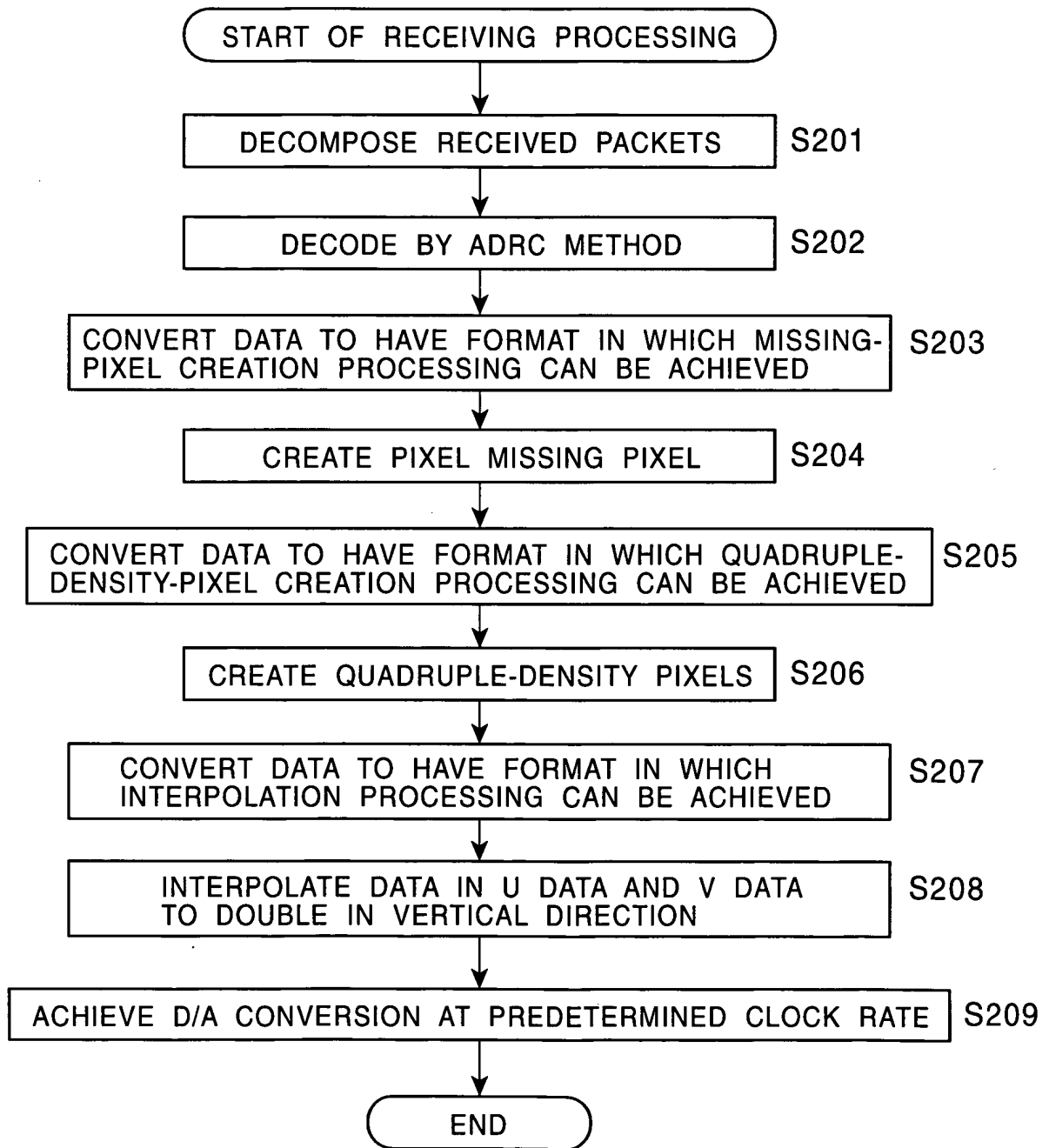


FIG. 70

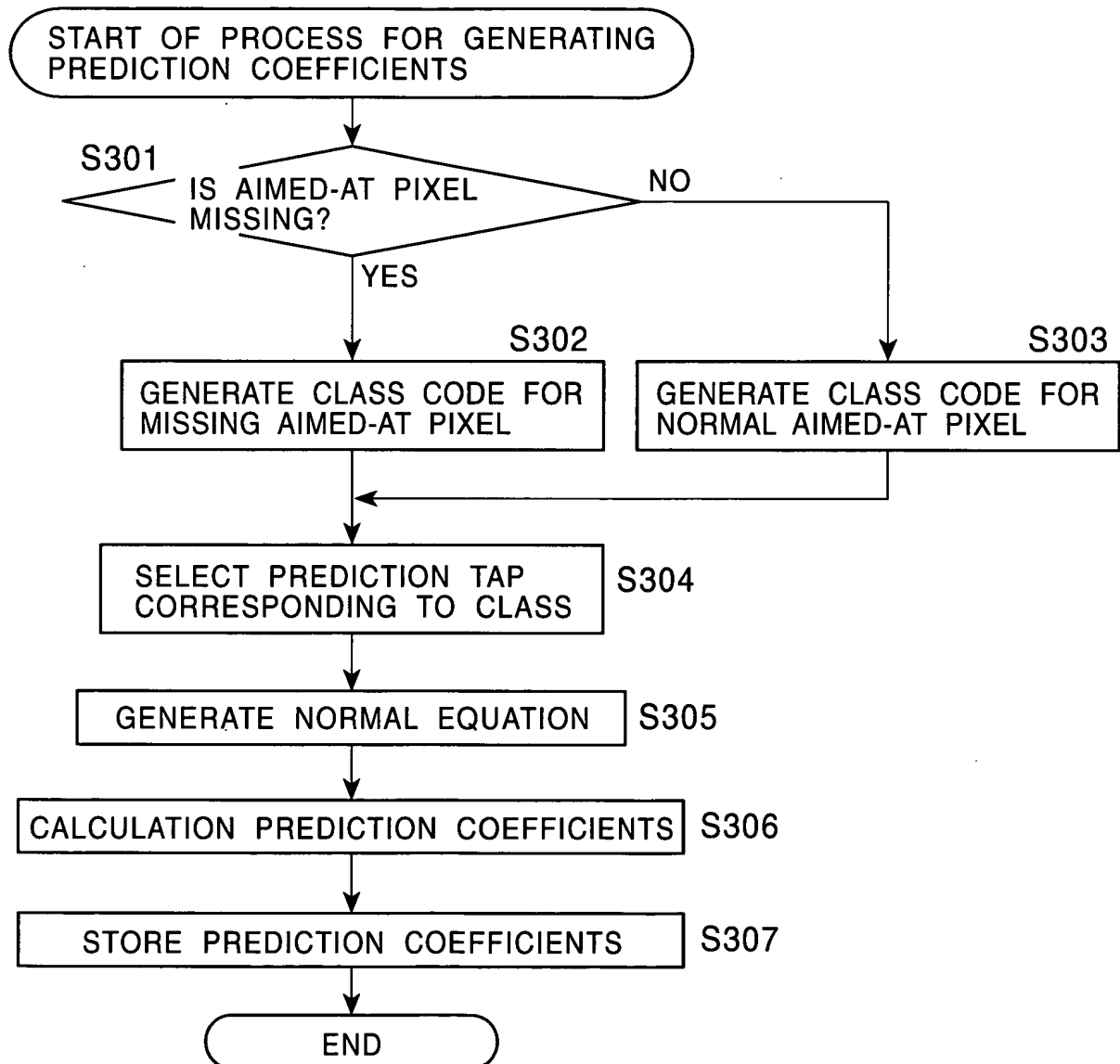


FIG. 71

